T.G.M. Z3

SM202

Timer Counter Series SM202

Instruction Manual

THIS SPECIFICATION IS APPROVED
FOR USE IN THE CALIBRATION OF
COMPANY INSTRUMENTS.
(2)
CALIBRATION DEPARTMENT
QC FACILITIES
DATE: 6-1-81
BRITISH AIRCRAFT CORPORATION, STEVENAGE.

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Instruction Manual

TIMER/COUNTER

SERIES

SM 202

Issue 2

February 1973

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LIST OF AMENDMENTS

Al.No.	By Whom	Date

Al.No.	By Whom.	Date.

PREFACE

DAMAGE IN TRANSIT

Unpack the equipment and examine it thoroughly to ascertain whether any damage has occurred in transit. Report immediately any such damage to the agent or manufacturer. Retain the four rubberized packing surrounds, should a return to manufacturer be necessary.

GUARANTEE

2. All goods manufactured by the Company are guaranteed to the extent hereafter mentioned against defects arising from faulty material or workmanship subject to the goods not having suffered maltreatment or interference. The Company's liability under this guarantee is limited to replacing any part or parts found defective within a period as laid down in Company instructions after the date of delivery or installation.

If goods not of the Company's manufacture are ordered, the guarantee of that company is to be accepted.

LOCAL AGENTS ADDRESS:-

The address of your local agent is:-

DESCRIPTIVE MATTER AND ILLUSTRATIONS.

Descriptive matter, illustrations, dimensions and weights issued by the Company are typical and shall not be held as binding. The Company reserves the right to alter patterns and designs without notice.

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SECTION 1

SPECIFICATION

TIMER/COUNTER SM 202

Display:

Eight side-view numerical indicator tubes with integral decimal points.

Stored or non-stored display, selected by front panel push-button.

Display time is variable by front panel control between 0 and 3s, in frequency, period and average period.

2 side-view, character indicator tubes display units of kHz, MHz, μs, ms, and sec as appropriate.

Full Scale Count:

99999999 plus overrange indication when full scale is exceeded.

Maximum Time Resolution:

100ns

A Input:

(i) *Maximum Sensitivity:* 10 mV r.m.s.

(ii) *Input Impedance:* 1MΩ in parallel with < 20 pF.

(iii) *Maximum Amplitude:* 300 V r.m.s. at 50 Hz.

(iv) *Frequency Range:* DC to 150 MHz at 50 mV r.m.s. (sinewave). In AC, lower r.m.s. (sinewave) In AC, lower frequency limit 10 Hz.
For pulse width limits see Section 3, Sub-section 8.

(v) *A Input Controls:* Front panel toggle switch selects a.c. or d.c. coupling. Four position front panel rotary switch selects 10 mV r.m.s., 100 mV r.m.s., 1 V r.m.s. and 10 V r.m.s. maximum sensitivity.
Front panel level control selects trigger point.

Range is ± 100 mV on 10 mV range, proportionately greater on attenuated ranges.

B Input and C Input:

(i) ***Maximum Sensitivity:*** 100 mV r.m.s.

(ii) ***Input Impedance:*** 1 MΩ in parallel with 20pF.

(iii) ***Maximum Amplitude:*** 300 V r.m.s. at 50 Hz on all ranges.

(iv) ***Frequency Range:*** DC to 10 MHz.

(v) ***B and C Input Controls:*** Three position front panel rotary switches select 100 mV r.m.s., 1 V r.m.s. and 10 V r.m.s. sensitivity. Front panel level controls select trigger point. Range is ± 1V on 100 mV ranges, proportionately greater on attenuated ranges.

External Clock Input:

Applied to C INPUT channel with EXT CLOCK push-button depressed. Specifications as for C INPUT above. When selected, B-C gating is inhibited.

Internal Clock Oscillator:

10 MHz crystal-controlled oscillator in a temperature stabilised oven with proportional control.

Accuracy:

Temperature coefficient (average) over −10°C to +50°C: 2 parts in 10^9 per °C.

Daily ageing rate: 3 part in 10^9

Long term stability: 1 parts in 10^6 per annum.

Hold Facility:

Operation of front panel push-button stops counter at the end of a measurement sequence and the reading is held.

Reset Facility:

Operation of front panel push-button resets counter and display to zero. Overrides variable display time. When the RESET push-button is released the instrument is enabled for a measurement so that this control may b

MANUAL CHANGE AL 1
for
TIMER/COUNTER MANUALS

SM 202, [redacted].

REASON FOR CHANGE

Change in stated specification of daily ageing rate and long term stability figures for crystals as follows:

SM 202, [redacted].

Amend specification figures to read:

Daily Ageing Rate: <3 parts in 10^9 per day (average over 10 days)

Long Term Stability: <1 part in 10^6 per annum.

SM 205

Amend specification figures to read:

Daily Ageing Rate: <6 parts in 10^8 per day (average over 10 days)

used in conjunction with HOLD for single shot operation.

External Program Facility: Operation of front panel push button with other buttons released, provides for external programming with optional SM248 fitted. Front panel neon indicator is illuminated.

Z Modulation Output: Rear panel mounted BNC connector provides an output which may be used with an oscilloscope to display trigger point.

Totalise Facility: Front panel push-button operating in count and time. Inhibits automatic reset when gate closes so that readings may be totalised.

1 MHz Clock Output: A rear panel mounted BNC connector provides a 1 MHz clock output, at standard TTL levels derived from the internal 10 MHz oscillator.

Range Selection: Seven front panel push-button switches. Ranges as specified in *Modes of Operation.*

Modes of Operation:

(i) Frequency Mode

Selected by front panel push-button switch. In this mode the instrument measures the frequency of a signal applied to the front panel A input in terms of the clock oscillator. Input characteristics are as for A channel input specification. Minimum pulse width 5 ns.

Range	Gate Time	Full Scale	Display
1	10 µs	9999999.9	MHz
2	100 µs	999999.99	MHz
3	1 ms	99999.999	MHz
4	10 ms	9999.9999	MHz
5	100 ms	999999.99	kHz
6	1 s	99999.999	kHz
7	10 s	9999.9999	kHz

Note: High frequency limit is 150 MHz minimum.

(ii) Period Mode

Selected by front panel push-button switch. A four-position front panel rotary switch selects:

Period + ve: measurement starts and (stops on

positive transitions.
Period - ve: measurement starts and stops on negative transitions.
Pulse width +ve: measurement starts on a positive transition and stops on negative.
Pulse width -ve: measurement starts on a negative transition and stops on positive.

Input characteristics are as for A channel input specification. Minimum pulse width for period measurements is 10ns and for pulse width 50 ns.

Range	Time Units	Full Scale Display
1	100 ns	9999.9999 ms
2	1 µs	99999.999 ms
3	10 µs	999999.99 ms
4	100 us	9999999.9 ms
5	1 ms	99999.999 s
6	10 ms	999999.99 s
7	100 ms	9999999.9 s

(iii) Average Period Mode

Selected by front panel push-button switch.

The time over a number of periods of the signal applied to Channel A is measured, the number being determined by the range selected. The display gives the average time for one period in micro-seconds. The upper frequency limit is 10MHz and minimum pulse width 50 ns.

Range	Number of Periods	Full Scale Display
1	1	9999999.9 µs
2	10	999999.99 µs
3	10^2	99999.000 µs
4	10^3	9999.9999 µs
5	10^4	999.99999 µs
6	10^5	99.999999 µs
7	10^6	99.999999 µs

(iv) Time Mode

Selected by front panel-push button switch. Time ranges and units are as for period mode.

Gating is controlled by inputs to the B and C channels and input characteristics and controls are as specified for these channels.

A three position front panel toggle switch for each channel gives control of gating transition polarity in two positions. The third position 'manual' gives equivalent manual operation, the switch being biased away from this position.
Gating Modes are as follows:-

B—B. Selected by front panel push-button.
Instrument measures time between consecutive voltage transitions of the same polarity on Channel B, or between consecutive manual operations.

B—C. Selected by front panel push-button.
Instrument measures time between transitions on Channel B (Start) and Channel C (Stop), or between equivalent manual operations. This mode is inhibited when the "External Clock" push-button is operated.

(v) Count Mode

Selected by front panel push-button switch. Instrument counts signals applied to Channel A. Input characteristics are as for frequency mode for a scaling factor of x1. For scaling factors of x10 or greater the upper frequency limit is 10 MHz and minimum pulse width 50 ns.

Scaling factors are as follows:

Range	1	2	3	4	5	6	7
Scaling Factor	1	10	10^2	10^3	10^4	10^5	10^6

Delay Time Control:

In time and count modes the variable Display Time potentiometer is used to control a variable delay time. Closing of the main gate is inhibited during the period of this delay, so that problems due to contact bounce etc., are eliminated. With the control fully anticlockwise the delay is zero.

Active Probe Socket:

A rear panel mounted 3-way socket provides

power to operate the S.E. Laboratories Active Probe Type SMA21 which has an input impedance of IMΩ in parallel with 7 p.F.

Power Requirements:

(i) *Voltage.* 230V ± 15% or 115V ± 15% (230V supplied as standard)

(ii) *Frequency range.* 45 Hz to 65 Hz

(iii) *Power consumption.* 25VA approximately

Operating Temperature Range:

$0^{o}C$ to $+50^{o}C$

Dimensions:

Front panel 13in (33cm) width x 3½in (8.9cm) height Depth 11in (28cm).

Weight:

12 lb (5½kg) approximately

2. TIMER/COUNTER SM 202PB

Specification as for SM 202 with the following additions:

BCD Output Facility:

From rear panel mounted 50 way socket. Outputs are positive logic, standard 7400TTL Levels:

8 decades in BCD	32 lines
Overrange	1 line
Range in BCD	3 lines
Mode in 1 of n	5 lines
Hold	1 line
External Clock	1 line
Gating Mode (Logic 1 for B–B, 0 for B–C)	1 line
Store	1 line
Totalise	1 line
External Programme	1 line
0V Reference	1 line
Print Command	1 line

To rear panel mounted 18 way plug. Inputs positive logic, standard 7400 TTL Levels. Inputs have a loading factor of 1:

Range Address in BCD	3 lines
Mode Address in 1 of n	5 lines
External Reset (Logic 1 to Reset)	1 line

Hold	1 line
External Clock Address	1 line
Gating Mode (Logic 1 for B–B, 0 for B–C)	1 line
Store	1 line
Totalise	1 line
0V Reference	1 line

NOTE:

In the remote programming mode the display and output store is not reset by "Reset" push-button or External Reset Signal. The main counter will be reset and the store updated at the end of a reading.

SECTION 2

GENERAL INFORMATION

1. INTRODUCTION

1.1 Timer/Counter SM 202 is a portable instrument designed to operate over a frequency range of d.c. to 150 MHz. MSI integrated circuits are incorporated providing a very high reliability. Measurements are displayed on 8 side-view numerical indicator tubes with integral decimal points, and the units are displayed on 2 side-view character tubes.

1.2 Three input channels are fitted, Input A, Input B and Input C. Sensitivity is controlled on Input A by a balanced attenuator that is switched by a four-position, front panel rotary switch and can be selected to be 10 mV, 100 mV, IV, or 10V r.m.s. Sensitivity on Inputs B and C is also controlled by balanced attenuators, switched by 3-position, front panel rotary switches and can be selected to be 100 mV, IV or 10V r.m.s. High noise rejection is a feature of the instrument, ensuring that it is not triggered in noisy environments. The sensitivity and level controls can be adjusted to ensure that the correct trigger points are selected.

1.3 A Z-modulation output is provided on the rear panel, which can be used to display the trigger point of the Input A signal on an oscilloscope.

1.4 Facilities to hold a reading indefinitely and to reset the instrument (manually or externally) are fitted and the display can be stored or non-stored as required. When the stored display is selected the reading is updated at the end of each counting sequence, presenting a non-blinking readout. With a non-stored display, the reading changes with each count made by the internal counting circuit, and thus is constantly changing. When the end of the counting sequence is reached the final reading is displayed until the start of the next counting sequence, when it is reset to zero.

1.5 An input voltage protection circuit is incorporated for all input channels; the maximum safe input which can be applied is 300 V r.m.s. at 50 Hz.

1.6 Range selection is made by seven push-button switches. Where a resolution in excess of full scale is required, the instrument can be used in the overrange condition. This is indicated by a front panel overrange lamp.

2. MODES OF OPERATION

2.1 The instrument has five modes of operation, which are selected by front panel mounted, push-button switches:

(a) ***Frequency Mode.*** In the frequency mode, the instrument measures the frequency of a signal applied to the A input, in terms of the internal clock oscillator, up to a maximum frequency of 150 MHz (typically 165 MHz). The accuracy is that of the clock oscillator ($\pm$ 1 count.) By operation of a front panel push-button, the instrument can measure frequency in terms of an externally connected clock oscillator, the frequency of which must lie within the limits d.c. to 10 MHz. A facility to hold a reading indefinitely is included by operation of a front panel push-button. This mode can also be used for ratio measurements.

FIG 2.1 TIMER / COUNTER SM 202

(b) *Period and Pulsewidth Modes.* With positive or negative period selected, the instrument measures the period of a signal applied to the A input in terms of the internal clock oscillator. With the positive or negative pulsewidth position selected, the corresponding pulse width is measured. An external clock oscillator can be used as in (a) above. Frequency and accuracy limitations are as for the Frequency mode. Time units are in seconds, or milliseconds, depending upon the range selected.

(c) *Average Period.* In the Average Period mode, the instrument measures the average period of a signal applied to the A input. The display indicates an average period measured over a series of periods up to 10^6 as determined by the range selectors. Time units are in microseconds. This mode can also be used for ratio measurements.

(d) *Time Mode.* In the Time mode, the instrument operates as an elapsed time meter with range selection as for the Period mode. The timing sequence is controlled by voltage transitions applied to the B input or B and C inputs, or manually by using the toggle switches on the front panel. Alternatively the timing sequence can be controlled by external remote contact closure operation. The Delay Time control can be adjusted to eliminate false readings, caused by contact bounce on either input.

(e) *Count Mode.* In the Count mode, the instrument counts the input signal applied to input A. The count is controlled in the same way as in the Time mode above. The Delay Time control operates as in Time.

2.2 Frequency ratio measurements can also be made by use of the external clock facility (although this is provided primarily to allow the instrument to operate from an external frequency standard). Measurements of frequency, period, average period and time can be made relative to any externally connected frequency within the limits of the external clock input.

3. POWER REQUIREMENTS

3.1 The instrument is capable of operating from a power source in the range 115 V, ± 15% or 230 V, ± 15%, at frequencies between 45 Hz to 65 Hz. The power consumption is approximately 25 VA. The method of altering the instrument to suit the local power voltage is given in *Section 3, Installation and Operation.*

4. REMOTE PROGRAMMING AND PRINTER OUTPUT FACILITIES

4.1 On Timer/Counter SM 202PB, a 50-way socket on the rear panel provides outputs suitable for driving a digital printer (such as SE LABORATORIES model type SM 250). Outputs available are listed in *Section 1, Specifications.*

4.2 Programming inputs are provided by an 18-way plug on Timer/Counter SM 202PB. Inputs available are listed in *Section 1, Specifications.* Both programming and printer facilities can be added to a basic SM 202 instrument by the fitment of Programming and BCD Output Unit SM 248. This can be supplied as a plug-in p.c. board with wired 50-way and 18-way connectors.

5. RACK MOUNTING KIT SM 210/R

5.1 The physical dimensions are such that the instrument can be used on the bench or rack mounted in standard 19 inch rack. The chassis is drilled to accept a rack mounting kit which is supplied as an optional extra.

SECTION 3

INSTALLATION AND OPERATION

1. INTRODUCTION

1.1 This section contains all the information necessary to install and operate the timer/counter.

2. UNPACKING

2.1 The instrument is supplied sealed in a polythene bag and is surrounded by rubber packing blocks. These should be retained for use again should further transportation be required.

3. EQUIPMENT LIST

3.1 The standard instrument is supplied with the following items:

(a) Miniature connectors, (for input A, B, C, IMHz clock and Z Mod Output sockets), plug BNC type GE 35070/C 12 (Greenpar) pt. no. AS 0450.

(b) Fuse link, 250 mA, type TDC 123 (20 mm x 5 mm), fitted.

(c) 50-way free plug (for BCD output facility), McMurdo MP 150 and short cover top entry McMurdo MC 150S (SM 202 PB only).

(d) 18-way free socket (for programming facility), McMurdo MS 118, and short cover top entry, McMurdo MC 118S (SM 202 PB only).

(e) Hinge plates, McMurdo ML/H (2 pr.) and locking plates, McMurdo ML/L, for connectors in (c) and (d) above.

(f) Instruction Manual.

(g) Carrying Case SM 210/C (optional at extra cost).

(h) Rack Mounting kit SM 210/R (optional at extra cost).

4. RACK MOUNTING

4.1 The SM 202 can be bench or rack mounted. Extensions are added to either side of the front panel so that it can be held in place in the rack. This system is available in kit form as an optional extra, and is shown in fig. 3.1.

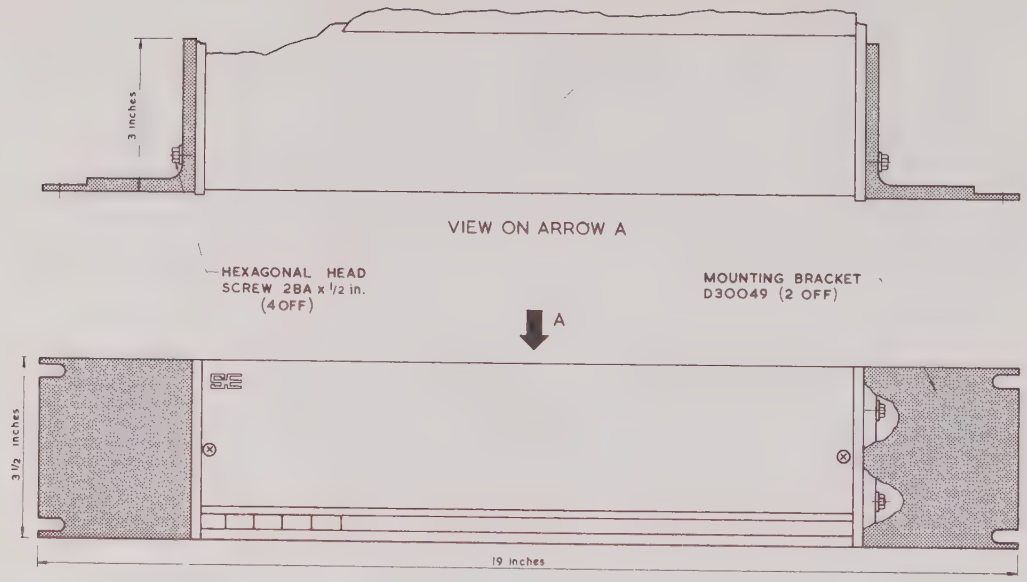


FIG. 3.1 RACK MOUNTING DETAILS

5. POWER SOURCE SELECTION

5.1 The timer/counter is supplied wired to accept the mains input voltage as specified by the customer. For 230 V operation, primary windings of T1 are connected in series, and for 115V operation, they are connected in parallel (See fig. 3.2). Unless specified, the instrument is connected for 230V.

CAUTION

Ensure that the instrument is isolated from the power source when changing the voltage tappings.

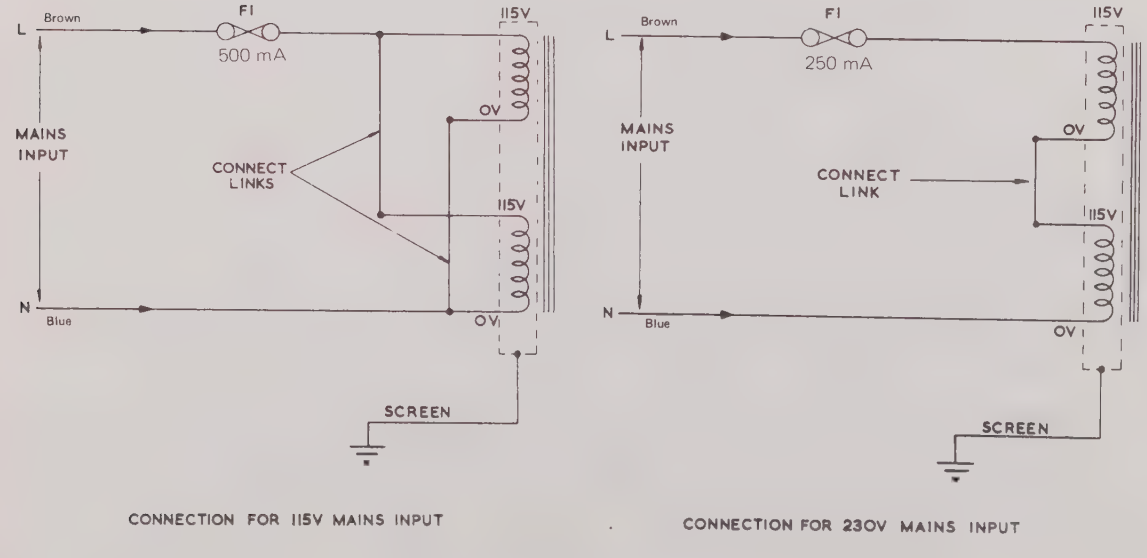


FIG. 3.2 POWER SOURCE SELECTION

6. CONNECTIONS

6.1 Power Lead

6.1.1 The power lead should be connected: Brown wire to Live, Blue wire to Neutral and Green/Yellow wire to Earth (ground).

6.2 BCD Output 50-way Socket (Rear Panel)

6.2.1 The pin connections and functions for the 50-way BCD output socket are listed below: the logic levels are:

Logic 1: +2.4V (min) to +5V (max)
Logic 0: 0 to +0.4V (max). Sink capability 10mA

(a) BCD Outputs

	DECADES PIN NOS.								
BCD Code	1	2	3	4	5	6	7	8	Overrange
8	D1	D2	D3	D4	D5	D6	D7	D8	A9
4	C1	C2	C3	C4	C5	C6	C7	C8	
2	B1	B2	B3	B4	B5	B6	B7	B8	
1	A1	A2	A3	A4	A5	A6	A7	A8	

(b) Range Outputs

	Pin Nos.		
Range	D9	C9	B9
	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

(c) Mode

	Pin Nos.	
Frequency	A10	Logic 1 denotes mode selected
Period	B10	
Average Period	C10	
Time	D10	
Count	A11	

(d) Other Functions

Function	Pin No.	Operative Logic State
Hold	B11	Logic 1
External Clock	C11	Logic 1
Gating Mode	D11	Logic 1 for B-B, Logic 0 for B-C
Store	A12	Logic 1
Totalise	B12	Logic 1
External Programme	C12	Logic 1
0V Reference	A13 C13	—
Print Command	D12	Logic 1 to Command Print

6.3 Remote Program 18 Way Plug (Rear Panel)

(a) Range Address

Range Address	Pin No. C1	B1	A1
	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

(b) Mode Address

	Pin No.	
Frequency	D1	Logic 1 denotes mode selected
Period	A2	
Av. Period	B2	
Time	C2	
Count	D2	

(c) Other Functions

Function	Pin No.	Operative Logic State
External Reset	A3	Logic 1
Hold	B3	Logic 1
External Clock Address	C3	Logic 1
Gating Mode	D3	Logic 1 for B-B, Logic 0 for B-C
Store	A4	Logic 1
Totalise	B4	Logic 1
0V Reference	C4, D4	—

6.4 Active Probe Socket

Function	Pin No.
+12V d.c.	1
-12V d.c.	2
0V	3

View from Front of Socket

7. SUMMARY OF CONTROLS, CONNECTORS AND INDICATORS

7.1 The controls, connectors and indicators located on the front panel are summarized as follows (see fig. 3.3):

(a) RANGE Switches and Units Indicator:

(i) ***1:*** Selects range up to full scale readings of:

Frequency:	9999999.9 MHz (max. freq. 160 MHz typical)
Period:	9999.9999 ms
Average Period:	9999999.9 µs
Count:	99999999
Time:	9999.9999 ms

(ii) ***10:*** Selects range up to full scale readings of:

Frequency:	999999.99 MHz (max. freq.160 MHz typical)
Period:	99999.999 ms
Average Period:	999999.99 µs
Count:	99999999 x 10
Time:	99999.999 ms

(iii) 10^2: Selects range up to full scale readings of:

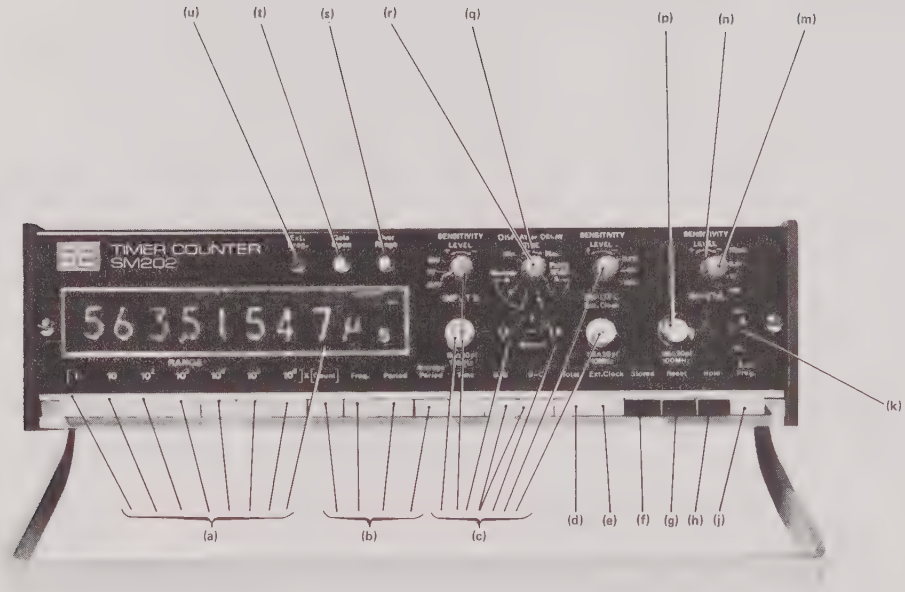
Frequency:	99999.999 MHz
Period:	999999.99 ms
Average Period:	99999.999 µs
Count:	99999999 x 10^2
Time:	999999.99 ms

(iv) 10^3: Selects range up to full scale readings of:

Frequency:	9999.9999 MHz
Period:	9999999.9 ms
Average Period:	9999.9999 µs
Count:	99999999 x 10^3
Time:	9999999.9 ms

(v) 10^4: Selects range up to full scale readings of:

Frequency:	999999.99 kHz
Period:	99999.999 seconds



(a) Ranges Switches and Units Indicator

(b) Mode Select Push-buttons

(c)Time and Count Gating Controls

(d) Total Push-button

(e) External Clock Select Push-button

(f) Stored Display Select Push-button

(g) Reset Display Push-button

(h) Hold Display Push-button

(j) External Programme Select Push-button

(k) Coupling Switch

(m) Input A Level Control

(n) Input A Sensitivity Switch

(p) Input A Connector

(q) Period/ Pulsewidth Polarity and Mode Switch

(r) Display or Delay Time Control

(s) Overrange Indicator

(t) Gate Open Indicator

(u) External Programme Indicator

FIG 3.3 CONTROLS, CONNECTORS AND INDICATORS – FRONT PANEL

Average Period: 999.99999 µs
Count: 99999999 x 10^4
Time: 99999.999 seconds

(vi) *10^5*: Selects range up to full scale readings of:
Frequency: 99999.999 kHz
Period: 999999.99 seconds
Average Period: 99.999999 µs
Count: 99999999 x 10^5
Time: 999999.99 seconds

(vii) *10^6:* Selects range up to full scale readings of:
Frequency: 9999.9999 kHz
Period: 9999999.9 seconds
Average Period: 9.9999999 µs
Count: 99999999 x 10^6
Time: 9999999.9 seconds

(viii) *Units Indicator:* 2 side-view character indicator tubes automatically display units of kHz, MHz, µs, ms and sec as appropriate.

(b) Mode Select Push-buttons: (see (a) for ranges.)

(i) *COUNT.* Selects Count mode.

(ii) *FREQ.* Selects Frequency mode, readings displayed in MHz or kHz, of signal applied to INPUT A.

(iii) *PERIOD.* Selects Single Period mode to give readings in milliseconds or seconds. Used in conjunction with the PERIOD A + −: PULSE WIDTH + − switch (d).

(iv) *AVERAGE PERIOD.* Selects Average Period mode to give readings in microseconds.

(v) *TIME.* Selects Time mode. Can be used with B-C gating. For alternative method of pulse width measurement (see Para. 8.6.2).

(a) INPUT B Channel

(c) Time and Count Gating Controls and Connectors:

(i) *B-B Push-button:* 'Start' and 'stop' for Time and Count modes gated from INPUT B signal.

(ii) ***INPUT B Connector:*** Gating signal for B channel connected here, maximum input 300V r.m.s. at 50 Hz.

(iii) ***B + —: MANUAL Switch:*** Selects method of 'start:stop' facility.

(iv) ***SENSITIVITY Switch:*** 3-position rotary switch selects input B sensitivities of 100 mV r.m.s., 1V r.m.s., and 10V r.m.s. A concentric LEVEL control can be adjusted to select the trigger point on the input B waveform.

(b) INPUT C Channel

(i) ***B-C Push-button:*** 'Start' and 'stop' for Time and Count modes
'Start' on INPUT B signal
'Stop' on INPUT C signal

(ii) ***INPUT C Connector:*** Gating signal to stop Time and Count modes (in B and C gating) connected here, maximum input 300V r.m.s. at 50 Hz. External clock input is also applied here with EXT. CLOCK push-button depressed. **NOTE:** B—C start/stop in time and count modes is inhibited when EXT CLOCK is selected. B—B gating is not affected.

(iii) ***C + —: MANUAL switch:*** Selects method of 'start/stop' facility.

(iv) ***SENSITIVITY Switch:*** 3-position rotary switch selects input C sensitivities of 100 mV r.m.s., 1V r.m.s., and 10V r.m.s. A concentric LEVEL control can be adjusted to select the trigger point on the input C waveform.

(d) TOTAL Push-button: When depressed, the automatic reset (which normally occurs when the gate closes) is inhibited and the next count starts from the previous counted value. The totalise facility only operates in the time and count modes.

(e) EXT CLOCK Push-button: When selected inhibits internal clock operation, so that

the instrument can be driven from an external oscillator (d.c. to 10 MHz). It can be used on all modes, the input is applied to the INPUT C connector.

(f) STORED push-button:

When the push-button is depressed, the instrument operates in the 'stored' mode and the display is updated at the end of each measurement sequence.

When the push-button is released the display follows the main counter during the measurement sequence and holds the reading until the next reading is initiated.

(g) RESET Push-button:

When depressed, it resets the display to zero except when EXT PROG is selected. When released, the instrument can take further measurements as selected by other controls.

(h) HOLD Push-button:

This facility operates in any mode. When selected, inhibits automatic resetting of the instrument at the end of a measurement sequence, thus displaying the last measurement made (until the instrument is reset manually or by the external reset signal).

(j) EXT PROG Push-button and Indicator:

When depressed, and with all other push-buttons released, selects external programme mode. In this mode, the instrument cannot be reset by the RESET push-button or an external reset signal. When external programme mode is selected, the EXT PROG Indicator is illuminated.

(k) INPUT A Coupling Switch:

(i) A.C. This position is selected if the d.c. component of the input signal exceeds the range of the trigger level control on the range selected. Lower frequency limit for input is 10Hz.

(ii) D.C. On this position, the frequency range is d.c. to 100 MHz (with full sensitivity) or 150 MHz (at 50 mV r.m.s. sensitivity).

(m) INPUT A LEVEL Control:

This control is adjusted in conjunction with the INPUT A SENSITIVITY switch to obtain the correct trigger point on the signal to be measured.

(n) INPUT A SENSITIVITY Switch:

Four-position switch, with the most sensitive position at the 10 mV r.m.s. range. Having selected the sensitivity,

the INPUT A LEVEL control is adjusted for correct trigger point if necessary.

(p) INPUT A Connector: The 'signal to be measured' is connected here for all modes except Time mode.

(q) PERIOD A + – : PULSEWIDTH A + – Switch: This switch is used in the PERIOD mode to select the polarity of the signal as follows:

(i) ***Period + :*** The period of a signal on INPUT A is measured, with the measurement starting and stopping on positive transitions.

(ii) ***Period –:*** The period of a signal on INPUT A is measured, with the measurement starting and stopping on negative transitions.

(iii) ***Pulsewidth +:*** The pulse width of a positive going pulse on INPUT A is measured.

(iv) ***Pulsewidth –:*** The pulsewidth of a negative going pulse on INPUT A is measured.

(r) DISPLAY OR DELAY TIME Control: This control is concentric with the PERIOD A + –: PULSEWIDTH A + – control and has two uses:

(i) ***Frequency, Period, Average Period Modes.*** In these modes, the display time can be varied from 0 to 3 seconds. At fully anti-clockwise, the display time is 0.

(ii) ***Time and Count Modes.*** In these modes, the closing of the main gate can be delayed from 0 to 60 ms by this control. This affects the start signal on INPUT B only and is used to eliminate spurious signals caused by contact bounce. The first contact closure initiates the start signal and subsequent 'contact-closure signals' caused by bounce are inhibited for a time duration set in by the DELAY time control. In a condition like this, the INPUT C line should be used to stop the count. At fully anti-clockwise, the delay time is 0.

(s) OVER RANGE Indicator:

When lit, this lamp indicates that the value of the reading displayed is higher than the capacity of the main counter. The instrument can be used in the 'overrange' condition to obtain a higher resolution than that given by the significant digits available, provided that the non-displayed (most significant) digits are known, by first taking a measurement at a shorter gate time. This increases the effective resolution.

(t) GATE OPEN Indicator:

When lit, this lamp indicates that the instrument is taking a measurement. During unlit periods, the instrument is updating readings and resetting counting circuits ready for the start of the next count or sequence.

(u) EXT PROG Indicator:

Refer to Para. 7.1 (j).

7.2 Connectors and switches located on the rear panel are as follows (fig. 3.4):

(a) POWER ON Switch:

At ON, power is supplied to the whole instrument and the numerical indicator tubes display all 0 at switch-on.

(b) 1 MHz CLOCK OUTPUT Socket:

This BNC socket provides a 1 MHz clock output at standard TTL logic levels, derived from the internal 10 MHz oscillator.

(c) Z MOD OUTPUT socket:

This BNC socket provides a Z modulation output of the INPUT A signal, for display on an oscilloscope, so that the correct trigger point can be accurately set, using the INPUT A LEVEL control.

(d) ACTIVE PROBE SUPPLY Socket:

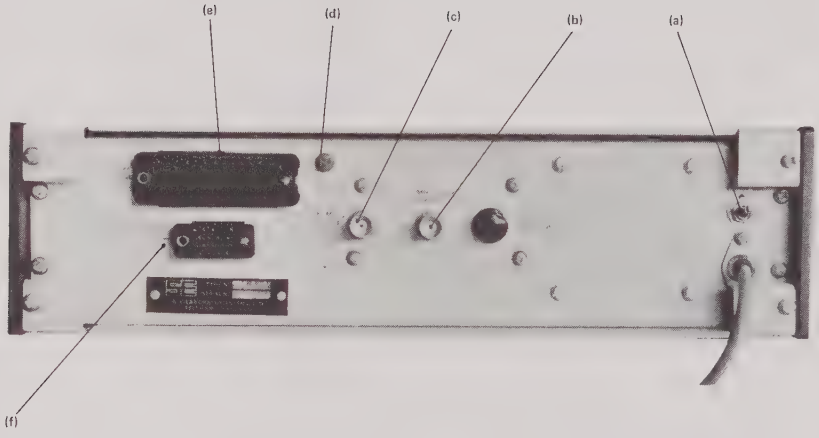
This socket provides ± 12V d.c. supplies for use with the SMA 21 Active Probe. Use of this probe reduces the input capacity to 7 pF, without insertion loss, or, provides an input of 10 MΩ at 10 pF with 10:1 insertion loss (in both instances at 120 MHz bandwidth).

(e) PRINTER OUTPUTS Socket:

This is a rear panel mounted 50 way socket. Outputs are positive logic, standard 7400TTL Levels.

OUTPUTS

8 decades in BCD	32 lines
Overrange	1 line
Range in BCD	3 lines
Mode in 1 of n	5 lines
Hold	1 line



(a) Power Switch

(b) 1 MHz Clock Output Socket

(c) Z Modulation Output Socket

(d) Active Probe Supply Socket

(e) Printer Output Socket

(f) External Programme Input Plug

FIG 3.4 CONTROLS AND CONNECTORS – REAR PANEL

External Clock	1 line
Gating Mode	1 line
Store	1 line
Totalise	1 line
External Programme	1 line
0V Reference	1 line
Print Command	1 line

For pin connections and operative logic states see Para. 6.2.

(f) EXTERNAL PROGRAM INPUTS Plug: This is a rear panel mounted 18 way plug. Inputs positive logic, standard 7400 TTL Levels. Inputs have a loading factor of 1.

INPUTS

Range Address in BCD	3 lines
Mode Address in 1 of n	5 lines
External Reset	1 line
Hold	1 line
External Clock Address	1 line
Gating Mode	1 line
Store	1 line
Totalise	1 line
0V Reference	1 line

For pin connections and operative logic states see Para. 6.3.

8. OPERATING INSTRUCTIONS

The following procedures are correct assuming the internal clock oscillator is being employed. External clock operation and the use of the LEVEL and SENSITIVITY controls are described under separate headings. The effects of noise on incoming waveforms are dealt with under *Application Notes.*

8.1 Preliminary Checks and Precautions

(a) If the instrument has been in store for a prolonged period, check for evidence of dampness before switching-on. If damp, dry out with warm, dry air.

(b) For normal use, the instrument should be grounded. However, if the mains frequency is to be measured it is important to ensure that excessive currents do not flow in the input low line. This

can be done in one of two ways:—

(i) using an isolating transformer across the INPUT A connector.

(ii) resistively coupling the INPUT A high side to mains live (1MΩ) and selecting the highest range. No connection is required to the INPUT A low side.

8.2 Frequency Measurement

8.2.1 In this mode, the instrument measures the frequency of a signal applied to the front panel INPUT A connector in terms of its internal clock oscillator. The maximum sensitivity is 10mV r.m.s. Frequency limits are between d.c. and 100 MHz at full sensitivity and d.c. to 150 MHz at 50mV r.m.s. Minimum pulsewidth is 5nsecs. With a.c. input coupling, the lower frequency limit is 10Hz. The maximum input voltage is 300V r.m.s. at 50 Hz on all input ranges.

(a) Connect the signal to be measured to INPUT A.

(b) Set the controls as follows:

(i) Depress the FREQ push-button

(ii) Depress the STORED push-button. For normal operation in the Frequency mode, the instrument is used with the 'stored-display' facility, the reason being that the period of stable display is very short, and with non-stored selected, the display would appear as a 'multi-glow' reading.

(iii) Ensure that the EXT CLOCK push-button is not depressed.

(iv) Select the highest (frequency) range push-button (when the frequency is unknown) and then 'range-down' until sufficient resolution is obtained:

Range (left to right)	Gate Time	Full Scale Reading
1	10 µs	9999999.9 MHz (see note)
2	100 µs	999999.99 MHz (see note)
3	1 ms	99999.999 MHz (see note)
4	10 ms	9999.9999 MHz (see note)
5	100 ms	999999.99 kHz
6	1 s	99999.999 kHz
7	10 s	9999.9999 kHz

NOTE: In FREQ mode, the high frequency limit is 150 MHz, typically 165 MHz.

(v) Adjust the INPUT A LEVEL and SENSITIVITY controls if necessary (see ***Application Notes***).

(c) To hold a reading, press the HOLD push-button. To obtain a new reading press and release the RESET push-button. Operation of the RESET push-button resets the counter circuit and display to zero. A new reading is initiated when the push-button is released.

8.3 Single Period and Pulsewidth Measurement

8.3.1 The period or pulsewidth of a signal applied to INPUT A is measured in terms of the internal clock oscillator. The frequency limit is 10Hz to 10MHz. With pulsewidth measurement, the minimum pulsewidth is 50ns. With period measurement the minimum pulsewidth is 10ns.

(a) Connect the signal to be measured to INPUT A.

(b) Set the controls as follows:

(i) Depress the PERIOD push-button. Select ac input coupling only if the d.c. component of the input signal exceeds the range of the trigger level control on the range selected.

(ii) Set the PERIOD A: PULSEWIDTH A switch to the type of measurement required (see fig. 3.5).

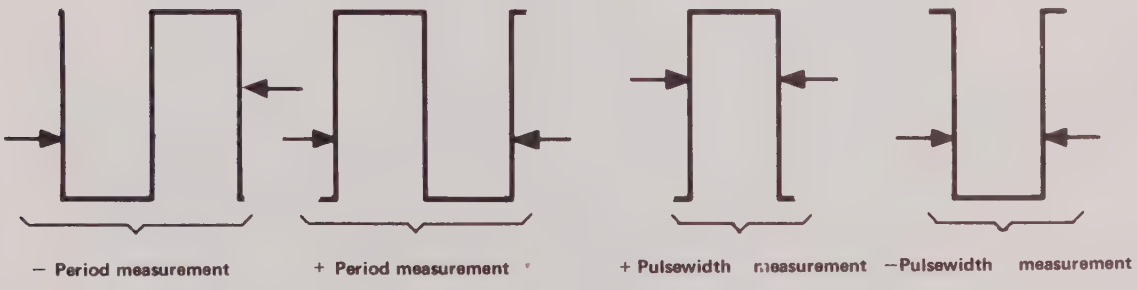


FIG. 3.5 PERIOD AND PULSEWIDTH MEASUREMENT

(c) Select the appropriate range:

(i) When only the frequency is approximately known (amplitude unknown) select the relevant range push-button and adjust the INPUT A LEVEL and SENSITIVITY controls, if necessary (see *Application Notes).*

(ii) When the frequency of the input signal is unknown, select range 1 and then 'range down' until the required resolution is obtained.

Range (left to right)	Time Units	Full Scale Reading
1	100 ns	9999.9999 ms
2	1 µs	99999.999 ms
3	10 µs	999999.99 ms
4	100 µs	9999999.9 ms
5	1 ms	99999.999 s
6	10 ms	999999.99 s
7	100 ms	9999999.9 s

NOTE: Pulsewidth can be also measured by selecting the Time mode and using the Time and Count gating controls (see Para 8.6.2).

8.4 Average Period Measurement

8.4.1 In this mode, the time over a number of periods is measured, the number being determined by the range selected. By the positioning of the decimal point,the display then gives the average time for one period in microseconds. Frequency and pulsewidth limits are as for period:

(a) Connect the signal to be measured to INPUT A.

(b) Depress the AVERAGE PERIOD push-button.

(c) Select the appropriate Range:

Range (left to right)	Number of Periods	Full Scale Reading (µs)
1	1	9999999.9
2	10	999999.99
3	100	99999.999
4	1000	9999.9999
5	10000	999.99999
6	100000	99.999999
7	1000000	9.9999999

(d) Adjust the INPUT A LEVEL and SENSITIVITY controls if necessary (see ***Application Notes).***

8.5 Count Measurement

8.5.1 In this mode, the instrument counts signals applied to INPUT A. The frequency limits to which the instrument is capable of counting varies with the range selected (150 MHz for range 1 and 10 MHz for all other ranges). Frequency and pulsewidth limits are as for frequency mode on range 1 and as for period on other ranges. Set the controls as follows:

(a) Depress the COUNT push-button and select the appropriate range.

NOTE: The count is divided by the number engraved above the selected range button (e.g. the 10^3 range push-button divides the count by 1000. To obtain the ***true*** count value multiply by 10^2, 10^3, etc.)

(b) To totalise, depress the TOTAL push-button. At the end of the first count (or the count in progress) the display retains the counted value (instrument is not reset) and the next count is added to it.

(c) One of three methods can now be used to start and stop the count. These are described in Para. 8.7, ***Time/Count Gating Controls.*** Adjust the LEVEL and SENSITIVITY controls, if required (see ***Application Notes).***

8.6 Time Measurement

8.6.1 In this mode, the instrument operates as an elapsed time meter with ranges selected in the same way as for the single period measurement (Para. 8.3):

(a) Depress the TIME push-button and select the range. The ranges for this mode are as shown below:

Range (left to right)	Time Units	Full Scale Reading
1	100 ns	9999.9999 ms
2	1 µs	99999.999 ms
3	10 µs	999999.99 ms
4	100 µs	9999999.9 ms
5	1 ms	99999.999 s
6	10 ms	999999.99 s
7	100 ms	9999999.9 s

(b) One of three methods can now be used to start and stop the timing sequence. These are described in Para. 8.7, ***Time/Count Gating Controls.***

(c) To totalise, depress the TOTAL push-button. At the end of the first count, the display retains the counted value, and the next count is added to it.

8.6.2 ***Pulsewidth Measurement.*** The time mode can also be used to measure pulse width as follows:

(a) Connect the signal to be measured to the INPUT B and INPUT C connectors (linked together).

(b) Depress the B-C push-button.

(c) Set the + −: MANUAL toggle switches as follows:

(i) INPUT B to +

(ii) INPUT C to −

(d) Depress the TIME push-button and select the appropriate range. The pulsewidth is measured as shown in fig. 3.6. The positions of the toggle switches can be reversed to measure a negative - going pulse.

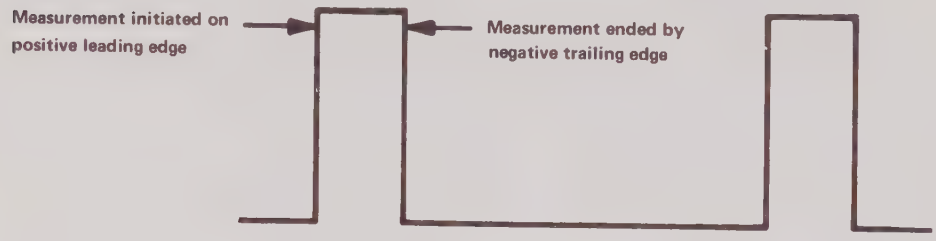


FIG. 3.6. TIME MODE – PULSEWIDTH MEASUREMENT

8.7 Time and Count Gating Controls

8.7.1 The interval that is to be timed, or the interval during which signals on INPUT A are to be counted, can be controlled electrically or manually using the + – MANUAL switches and INPUTS B and C where appropriate. One of two methods can be employed:

(a) **Method 1 : Manual Start:Stop** In this mode, the INPUT B and INPUT C connectors are ***not*** used.

(i) Select B-B push-button.

(ii) Start count (or timing sequence) by pressing associated + : – : MANUAL switch to MANUAL.

(iii) Stop count (or timing sequence) by pressing to MANUAL a second time.

– OR –

(i) Select B-C push-button

(ii) Start count (or timing sequence) by pressing (and releasing) + : – : MANUAL switch to MANUAL (associated with INPUT B channel).

(iii) Stop count (or timing sequence) by pressing (and releasing) the + : – : MANUAL switch to MANUAL (associated with the INPUT C channel).

(b) **Method 2: Signal Operated Start:Stop.** With this method, the count (or timing sequence) can be controlled by using one of the two gating modes:

(i) Gating Mode B-B: The count (or timing sequence) is started ***and*** stopped by a signal applied to the INPUT B connector provided the B-B push-button has been selected. The instrume

counts the number of signals or time units on INPUT A between consecutive voltage transitions of the ***same*** polarity on INPUT B. The operative transition can be of either polarity and is selected by the + : — : MANUAL switch associated with the INPUT B channel. The required input sensitivity for INPUT B is selected and the trigger point is set by the INPUT B LEVEL control.

(ii) ***Gating Mode B-C:*** The B-C push-button is selected. The count (or timing sequence) is started by a signal applied to the INPUT B connector and is stopped by a signal applied to the INPUT C connector. The instrument counts the number of signals or time units on INPUT A between a voltage transition on the INPUT B connector and one on the input C connector. The polarity of the operative transition can be selected by the + : — : MANUAL switch associated with the INPUT B-C channel. The input sensitivity and trigger point for each channel is set by the SENSITIVITY and LEVEL controls, respectively, associated with the relevant channel.

NOTE: If the B and C signals are derived from mechanical relays and switches to eliminate spurious start signals (due to contact bounce), the closing of the main control gate can be delayed from 0 up to 60 ms (approx) by the DELAY TIME control. The first touch of the contact-closure initiates the start signal and subsequent closures caused by bounce are inhibited for the time duration set-in by the control.

With these conditions, the INPUT C line should be used to stop the count. At the fully anti-clockwise position of the control, the delay is 0.

8.8 External Clock Operation

8.8.1 When an externally derived clock oscillator is to be used to drive the instrument, the EXT CLOCK push-button on the front panel must be selected and the external clock input should be applied to the INPUT C connector on the front panel. The frequency limit is d.c. to 10 MHz. In all other aspects, the instrument is then operated as for internal clock operation. The maximum amplitude is 300V r.m.s. at 50 Hz.

NOTE: With the EXT CLOCK push-button selected. the B-C time and count mode gating is automatically inhibited.

8.8.2 ***Calculation of Results.*** When the externally applied clock oscillator frequency is other than 10 MHz, the displayed reading of a measurement will be wrongly scaled. The calculation required to obtain the true reading differs, depending upon the measurement mode in use:

(a) **Period and Time Modes:**

$$\text{True Reading (seconds) (ms)} = \text{Displayed Reading (seconds) (ms)} \times \frac{10\ \text{MHz}}{\text{External Clock Frequency}}$$

(b) Average Period Mode:

$$\text{True Reading } (\mu s) = \text{Displayed Reading } (us) \times \frac{10\ \text{MHz}}{\text{External Clock Frequency}}$$

(c) Frequency Mode:

$$\text{True Reading } \frac{(kHz)}{(MHz)} = \text{Displayed Reading } \frac{(kHz)}{(MHz)} \times \frac{\text{External Clock Frequency}}{10\ \text{MHz}}$$

8.9 Ratio Measurements

8.9.1 *Frequency Mode.* The instrument is set-up as for the frequency mode using the external clock facility. The gate time is now controlled by the external oscillator frequency. Thus, if the external clock frequency is F_{ext} and the INPUT A frequency is Fi/p, the instrument reads:

$$10 \times \frac{Fi/p}{F_{ext}} \quad \text{on ranges 1, 2 and 3, 4}$$

$$\text{and} \quad \frac{Fi/p}{F_{ext}} \times 10^4 \quad \text{on ranges 5, 6 and 7}$$

NOTE: Both frequencies must be expressed in the same units.

8.9.2 *Period Mode.* The period of the INPUT A signal is measured in terms of the external clock oscillator period. The instrument reads (on all ranges):

$$\frac{F_{ext}}{Fi/p} \times 10^{-4} \quad \text{on ranges 1 to 4}$$

$$\frac{F_{ext}}{Fi/p} \times 10^{-7} \quad \text{on ranges 5, 6 and 7}$$

NOTE: Both frequencies must be expressed in the same units.

8.9.3 *Average Period Mode.* The instrument measures the average period of the signal applied to the INPUT A connector in terms of the external clock oscillator period. The instrument reads (on all ranges):

$$\frac{F_{ext}}{Fi/p} \times 10^{-1} \quad \text{on all ranges}$$

NOTE: Both frequencies must be expressed in the same units.

8.10 Hold and Reset Facility

8.10.1 To hold a reading in any mode, depress the HOLD push-button. A new reading can be obtained either by:

(a) pressing the RESET push-button (when the reading is reset to zero) then releasing it (when a new measurement sequence may start and this reading will be held) or

(b) application of a reset signal to the external reset input pin on the rear panel external program inputs socket; logic 0 (0 V to + 0.4 V) activates reset, logic 1 (+2.4 V to + 5 V) initiates a new measurement sequence.

9. APPLICATION NOTES

9.1 Effects of Noise on Frequency and Count Measurements

9.1.1 Excessive noise superimposed on the input signal can result in erroneous readings. The Input A LEVEL and SENSITIVITY controls should be adjusted, at the same time observing the signal input waveform on an oscilloscope (connected to Z MOD OUTPUT Socket) to obtain the best results. The effect of noise on the accuracy of the internal counting circuits is illustrated in fig. 3.7B.

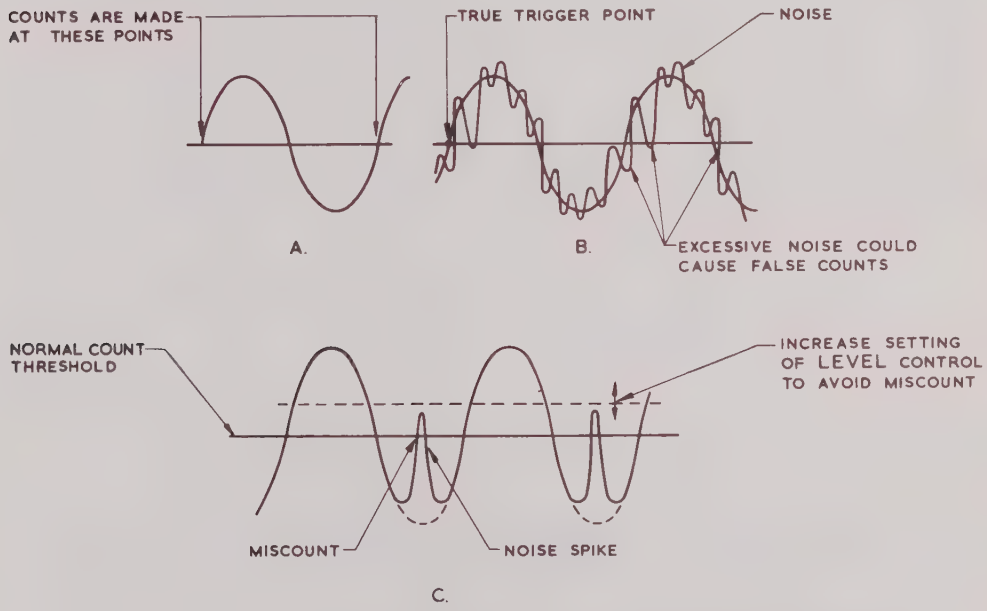


FIG. 3.7. NOISE ON FREQUENCY AND COUNT MEASUREMENTS

9.1.2 With a signal similar to that in fig. 3.7.B the SENSITIVITY switch should be used to attenuate the overall signal and the INPUT A LEVEL control adjusted so that the counter circuit is triggered at the correct point.

9.1.3 Miscounts can also be caused by the type of superimposed noise illustrated in fig. 3.7.C. To avoid this, increase the setting of the INPUT A LEVEL control. If the counting circuit is still miscounting, adjust the setting of the SENSITIVITY switch and re-adjust the LEVEL control, if necessary, observing the waveform on an oscilloscope.

9.2 Effects of Noise on Single Period Measurements

9.2.1 Where a small amount of external noise is present on the signal, an effect can occur where the noise triggers the counting circuit just prior to the true signal trigger point, as shown in fig. 3.8.

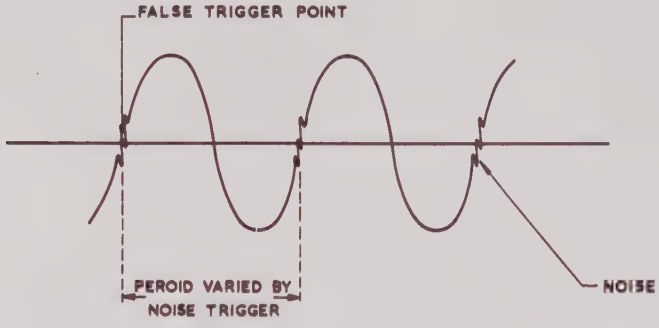


FIG. 3.8. NOISE ON SINGLE PERIOD MEASUREMENTS

This results in each period varying from the next in length, giving an overall "jitter" effect to the displayed reading. This can be reduced by using the AVERAGE PERIOD mode.

9.3 Pulsewidth Measurement

9.3.1 Inaccuracies in readings can occur where a sawtooth or ramp type pulse is being measured due to the effect shown in fig. 3.9.

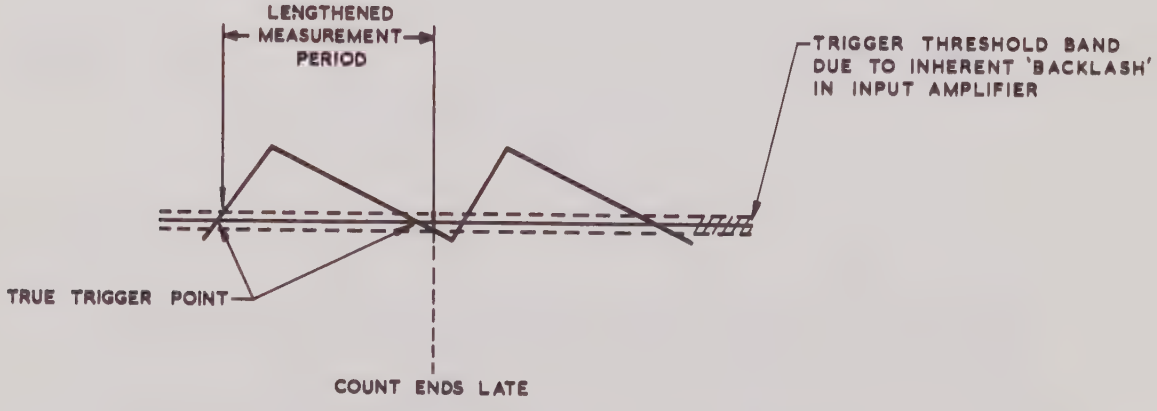

LENGTHENED MEASUREMENT PERIOD
TRIGGER THRESHOLD BAND DUE TO INHERENT 'BACKLASH' IN INPUT AMPLIFIER
TRUE TRIGGER POINT
COUNT ENDS LATE

FIG. 3.9. ERRORS ENCOUNTERED WITH RAMP INPUT WAVEFORMS

9.3.2 This effect occurs only when a marked difference exists between the rise and fall times of a waveform such as found with a ramp. From fig. 3.9 it can be seen that the instrument is measuring a longer period than actually exists. A longer delay before counting stops is caused by the more gradual slope of the trailing edge than was experienced with the leading edge to start the count. This can be minimised by setting the SENSITIVITY switch to the most sensitive setting to make the input signal as large as possible. The LEVEL control should be ideally set to the mean of the pulse.

SECTION 4

TECHNICAL DESCRIPTION

1. INTRODUCTION

1.1. Timer/Counter SM 202 for purposes of circuit description, can be considered as seven major sub-assemblies:

(a) **Input Amplifier Board.** This contains the signal input (input A) amplifier and the first decade (units) of the counting circuit. The first stage of the second counting decade is also mounted on this board.

(b) **Display and Logic Board.** This contains:

(i) the remaining decades of the counter and the associated stores, decoders and numerical indicator tubes.

(ii) units display logic

(iii) variable delay/display logic

(iv) control logic, time base (divider) and range selection logic, time and count mode gating logic and polarity selection gates.

(v) B and C channel input amplifiers.

(c) **Switch Board Assembly.** This provides the interconnections between the push-button switches and the display and logic board.

(d) **Front Panel Assembly.** All operator controls (except the POWER ON switch and push-buttons) are mounted on this assembly.

(e) **Rear Panel Assembly.** On this is mounted the printer and program connectors and clock sockets, mains fuse and POWER ON switch.

(f) **BCD Fan Out and Ext Programme Unit SM248.** This comprises a p.c. board, an 18-way and a 50-way connec The p.c. board carries a number of integrated circuit buffers for the BCD outputs, and logic gates for the overrange and print command functions and external programme facility.

(g) **Power Supply Unit.** This consists of the mains transformer and stabiliser circuitry.

1.2. A block schematic is shown in fig. 4.1.

2. INPUT AMPLIFIER (fig. 3.)

2.1. The input amplifier can be divided into 2 basic circuits as follows:

(a) input R–C attenuator with frequency compensation.

(b) a.c. amplifier and Schmitt trigger.

2.2. **The input attenuator** is formed by resistors R1 to R7 and capacitors C2 to C4; the resistors provide attenuation at low frequencies and the capacitors at high frequencies. The input signal is a.c. coupled by capacitor C1, with the input coupling switch open.

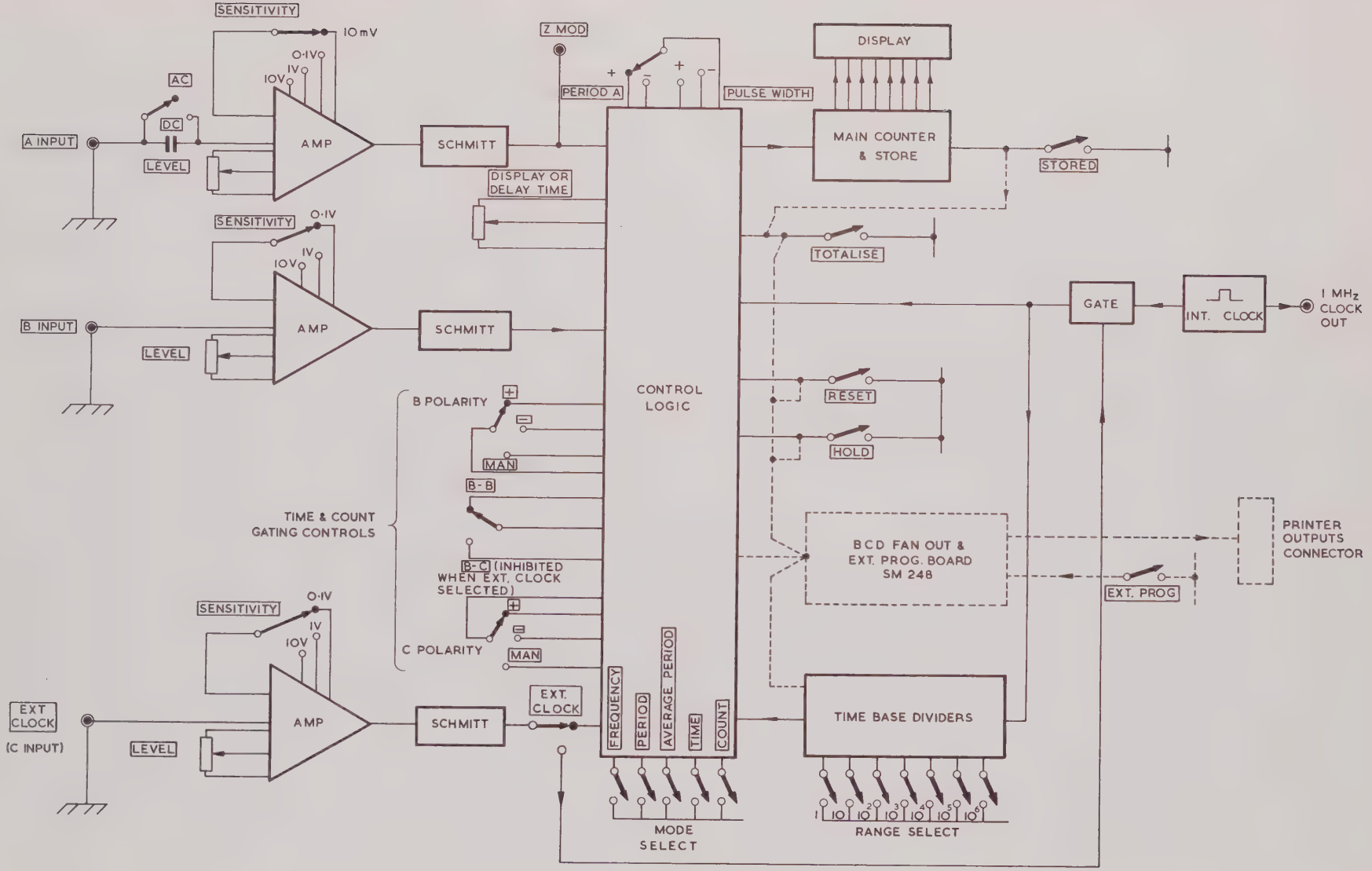


FIG. 4.1 SM 202 BLOCK SCHEMATIC

2.3. **A.C. Amplifier.** The a.c. signal is fed via the input attenuator and the limiter (D1, D2, R8, C5) to the base of source-follower TR1; the source follower is incorporated to provide a high input impedance. The source output of TR1 is applied to the base of TR2, which forms part of the long-tailed pair stage TR2, TR3, TR4, TR5 with constant current provided by R4 in the tail. The gain of the long-tailed pair is defined by resistors R18 and R20. The output of this stage is taken from the collectors via TR7 and TR8 to the Schmitt trigger stage TR9 and TR10. As the collectors of TR9 and TR10 are connected (via R34 and R37) to the 0V line and the emitters to the -5.2V line (via R36) the squarewave output (at the frequency of the output A signal) is between -0.7V and -2.0V (nominal values); these are the levels required for the counting logic mounted on the input amplifier board, and are applied via emitter follower TR11.

2.4. An offset current is also applied to TR5 base, via TR1 and TR6 by the LEVEL control RV1 which has the effect of moving the d.c. base line, about which the a.c. component alternates at TR7 collector.

2.5. Ferrite beads X1 to X4 are included as decoupling inductors to reduce effects of high-frequency noise.

3. DISPLAY AND LOGIC BOARD

3.1. The description of the logic on this board is given in terms of the modes of operation, with the control logic considered separately.

3.2. Frequency Mode (Fig 1 B)

3.2.1. In the frequency mode, the signal-to-be-measured is sampled for a set period of time, determined by the divider output selected by the range push-buttons.

3.2.2. The signal-to-be-measured is routed via the input amplifier circuit (fig. 3) to the clock input of bistable IC3/2 on the input amplifier board. It must be noted that this bistable is the first stage of the first decade of the counter, the remaining stages being IC7/1, IC7/15 and IC8. The output of bistable IC3/2 is fed into latching bistable IC5, the outputs of which are applied to gates IC6/15 and IC6/2.

3.2.3. Gate IC6/15 is enabled in the frequency mode, by depressing the FREQ push-button; the action is as follows. With FREQ depressed, a logic 1 is applied to gate IC10/3 (fig. 3.) The logic 0 output of gate IC10/3 enables gates IC6/15 and IC6/2 so that the incoming signal can be applied to the remainder of the 1st counter to produce 1, 2, 4, 8, outputs at pins 5a, 4a, 3a, and 2a respectively on the input amplifier board.

3.2.4. The length of time that the incoming signal is allowed to drive the counter is determined by the 'stop' input to the latching bistables IC5/12 and IC5/2 on the input amplifier board, (these are at logic 1 (0V) to enable).These are controlled by the output of the 'stop' bistable IC62/12, which in turn is governed by the selected divider 'X' output, of IC65 selected by the range switches.

3.2.5. The divider is fed with the 10MHz output pulse train of the clock oscillator, via gates IC39/3, 39/6, 38/3 to the first ÷ 10 divider element IC44. The divider chain comprises IC44, 46, 50, 53, 56, 61, 66 and 67 and the 1, 10, 10^2, 10^3, 10^4, 10^5, 10^6, and 10^7 outputs are applied to the range selection circuit IC65.

The A, B, C, inputs to IC65 are controlled by the Range switches and a truth table for these is given below, (see also the truth table for the units display logic on fig. 1A).

Range Selected	Logic states RA (1)	RB (2)	RC (4)
1	1	0	0
2	0	1	0
3	1	1	0
4	0	0	1
5	1	0	1
6	0	1	1
7	1	1	1

The inputs, D1 to D7, correspond to range 1 to 7, respectively, and one of these inputs is enabled according to the range code applied to pins A, B and C (the binary code corresponds to values 1 to 7). The selected output ('X' at pin 6) is routed via gate 1C49/6 to the 'gate open' bistable 1C60/6. The logic operation from this point is similar for all modes of operation and is described in ***Para. 3.7 Control Logic Sequence of Operation.***

3.3. Period and Pulsewidth Modes (Fig 1 C)

3.3.1. In the period mode, the instrument measures the period of the signal-to-be-measured in terms of the internal clock oscillator. With the front panel rotary switch set to positive or negative pulsewidth or period positions (and with the PERIOD push-button depressed), the corresponding pulsewidth or period of the signal is measured in terms of the internal clock oscillator.

3.3.2. The incoming signal is used to control the gate open logic, and the divider output is applied to the counting circuits.

3.3.3. The signal is routed via R41 and gates 1C2/10 (inverted) and 1C2/2 on the input amplifier board (fig. 3.) and both polarities are applied to the polarity selection gates of 1C68 on the display and logic board (fig. 1B)

3.3.4. The polarity selection gates are controlled by the +V and -V input functions fed from gates 1C73/10 and 1C73/13 respectively. These two gates are enabled by the $\overline{P}$ function (at logic 0), when the PERIOD A push-button is depressed. Depending upon the position of the PERIOD: PULSEWIDTH polarity switch, so depends the logic states of the outputs of gates 1C73/10 and 73/13. This is shown in the table below.

Switch Position	+V	−V	Polarity Gate Enabled
+V Period	1	0	68/3
−V Period	0	1	68/6
+ V Pulsewidth	1	0	68/3
- V Pulsewidth	0	1	68/6

3.3.5. The signal is then applied to the multi-input NOR gate 1C68/8, the output of which is applied as the clock input to the 'gate open' bistable 1C60/7. It is also applied to gate 1C55/11 which is enabled only on pulsewidth measurement. Pin 12 of gate 1C55/11 is at logic 1 (enabled) only during pulsewidth measurements (also in Time and Count modes), generated by gate 1C55/8. The inputs to gate 1C55/8 are both at logic 0 when the PERIOD/PULSE switch is on the PULSE positions. The logic operation from this point is similar for all modes of operation and is described in ***Para. 3.7 Control Logic Sequence of Operation.***

3.3.6. The clock oscillator output is applied to the third decade of the divider via gates 1C39/2, 39/6, 1C38/8 and 1C47/5. The 1, 10, 10^2, 10^3, 10^4, 10^5, 10^6, 10^7 outputs are applied to the range selection circuit 1C65. The selected 'X' output is fed via gate 1C49/2 and 1C49/8 and board pin 9a ($1/P_2$) to the input amplifier board. Here, it is applied to the clock input (pin 4) of bistable 1C4/1, which now forms the first stage of the first decade of the counter. Thus, the length of time that the counter is allowed to count is controlled by the period or pulsewidth duration of the incoming signal.

3.4. Average Period Mode (Fig 1 D)

3.4.1. In this mode, the instrument measures the average period of a signal applied to the A INPUT. The display indicates an average period measured over a series of periods up to 10^7 as determined by the range switches.

3.4.2. The signal-to-be-measured (amp O/P) is fed, via gates IC1/8 and IC2/2 on the input amplifier board (fig. 3), to gate 1C49/3 on the main logic board. This is enabled in the average period mode, so that the signal is fed via gate 1C47/8 to the divider decade. The selected 'X' output from the range selection circuit (see Para. 3.2.5.) is applied as the clock input to the 'gate open' bistable 1C60/6 via gate 1C49/6. From this point, the logic operation for the 'gate open & close' sequence is similar for all modes and is described in ***Para. 3.7 Control Logic Sequence of Operation.***

3.4.3. From this, it can be seen that the incoming signal is controlling the duration of the count. The counter is driven by the clock oscillator pulse train, which is routed via gates 39/2, 39/6, 49/11, 49/10 to bistable 1C4/1 on the input amplifier board. The network, R42, 43, 44 and D3 change the logic levels to be 0V for logic 1 and -5.2V for logic 0.

3.4.4. The 'stop' input to latch 1C5/12 is at logic 1 (0V) at this time, so that the output of bistable 1C4/1 is passed through to gates 6/3 and 6/14. These gates are enabled by a logic 0 (-5.2V) level fed from resistor R51.

3.5. Time Mode (Fig 1 E)

3.5.1. In this mode, the instrument operates as an elapsed time meter.

3.5.2. The internal clock oscillator pulse train is applied to the divider chain at pin 14 of 1C50, via the gate path 1C39/2, 39/6, 38/8 and 47/8. The outputs of the divider (1, 10, 10^2, 10^3, 10^4, 10^5, 10^6, 10^7) are applied to the range selection circuit (see Para. 3.2.5.) and the selected 'X' output is fed via gates 1C49/3 and 49/8 to bistable 1C4/1 on the input amplifier board. The network, R42, 43, 44 and diode D3 change the logic levels, so that a logic 1 is 0V and a logic 0 is -5.2V. This is the first stage of the first counter decade and the output is applied to the inputs of the latch bistable 1C5/12. In this mode, the 'stop' input is at logic 1 (0V) and the counter input is fed through to the channel select gates, of which 1C6/14 and 6/3 are enabled. The counter continues counting until the 'stop' bistable 1C62/12 (on the display and logic board) sets a logic 0 into the C (stop) input of bistable 1C5/12.

3.5.3. If a signal is connected to INPUT A during a time measurement it will not interfere with the logic operation as gates 1C43/3 and 1C68/6, 68/3, 16/2 on the display and logic board, are inhibited.

3.5.4. The duration of the count is controlled by the gating logic in the same way as for the count mode. See Para. 3.6.4.

3.6. **Count Mode (Fig 1 F)**

3.6.1. The count mode logic operation differs depending upon whether Range 1 is selected or not. The signal-to-be-measured is applied to the counting circuit, and the length of time that the counter is allowed to count is determined by the gate open (start) and close (stop) signal derived from the start/stop inputs (B and C).

3.6.2. **Range 1 Operation.** On range 1, the incoming signal-to-be-counted is applied directly from the input amplifier to the first bistable, IC3/2, of the first decade of the counter. On range 1, the depressed range 1 push-button connects board input pin 6a to logic 1 (with COUNT A also depressed) so that the channel select gates IC6/3 and IC6/14 are inhibited and gates IC6/15 and IC6/2 are enabled. The network R51, 52, 53 and D6 changes the logic levels so that a logic 1 is 0V and a logic 0 is -5.2V. Thus, the 1st decade of the counter starts counting.

3.6.3. **Range 2, 3, 4, 5, 6 and 7 Operation.** On these ranges, the incoming signal-to-be-counted is fed via gates IC1/8 and IC2/2 on the input amplifier board to gate IC43/3 on the main logic board. From here, it is fed via gate IC47/8 to the divider logic. The 10, 10^2, 10^3, 10^4, 10^5, 10^6 and 10^7 outputs from the divider are applied to the range selection circuit IC65 and depending upon the range selected, one output (D1 to D7) is fed via gate IC49/3 to IC4/1 on the input amplifier board.

3.6.4. **Gating Logic, B-B Gating Operation (fig. 4.3).** The B-B push-button is mechanically coupled to the B-C push-button, so that when the B-B push-button is depressed, it releases the B-C push-button. In this state, the j input pin of bistable IC64/7 is at logic 0 and the k input of bistable 64/12 at logic 1. This means that bistable 64/7 is inhibited, so that any spurious signals appearing on the 'C line do not affect the B-B operation. One of two methods of generating a start/stop (gate open/gate closed) signal can be used:

(a) ***Manual Gating on Input B.*** When the B POSITIVE: NEGATIVE: MANUAL; toggle switch is depressed to manual, input pin 5 of gate 58/6 is taken to 0V (pin 1 of gate IC58/3 at this instant being open-circuit) so that a negative going transition is generated at the output of exclusive OR gate 36/6 **(NOTE**: IC58/6 and gate 58/3 form a latch to prevent contact bounce effects when the switch is pressed). The transition on gate 36/6 clocks bistable 64/12 to produce a logic 0 output at $\overline{Q}$64/12. This output is twice inverted by gates 68/10 and 68/8 and applied as the clock input to 'gate-open' bistable 60/7. The output of bistable 64/12 is also fed to gate IC40/6 which forms part of the variable delay circuit.

(b) ***Signal Gating on Input B.*** When a signal on Input B is used to initiate the gating sequence, it is applied to pin 2 of exclusive OR gate 36/3 causing it to switch between 0V and +5V (approx.) For positive transient gating, (on Input B) input pin 1 of gate 36/3 is connected to logic 0 (0V) by the switch (at the + position). A positive transient (logic 1) on pin 2 of exclusive OR gate IC36/3 produces a logic 1 on pin 3. With the B + — MANUAL switch on +, a logic 0 is present on pin 6 of gate 58/6 resulting in a logic 1 on pin 5 of gate 36/6. Therefore, when the output of gate 36/3 goes to 1, gate 36/6 output drops to logic 0, clocking bistable 64/12. The truth table for a 2-input exclusive OR gate is given below.

For negative transient gating on Input B, input pin 1 of exclusive OR gate 36/3 is connected to 0V (logic 0) by the switch (at the — position). A negative transient (logic 0) appearing on pin 2 of gate 36/3 produces a logic 0 at its output (pin 3). With the B + — MANUAL switch at —, a logic 1 is present on pin 6 of gate 58/6, resulting in a logic 0 on pin 5 of gate 36/6. Therefore, when the output of gate 36/3 goes to logic 0, gate 36/6 output goes to logic 0, clocking bistable 64/12.

I/P 1	I/P 2	Output
1	1	0
1	0	1
0	1	1
0	0	0

TRUTH TABLE FOR 2-INPUT EXCLUSIVE OR GATE

3.6.5. **Gating Logic B-C Operation (fig. 1B).** When the B-C push-button is depressed, the J input of bistable 64/8 goes to logic 1 and the k input to bistable 64/12 goes to logic 0. When a start pulse appears on the B input line, $\overline{Q}$ 64/12 goes to logic 0, and stays on 0 even if other pulses are subsequently applied. When a stop pulse apppears on the 'C' line, Q64/8 changes to logic 0, resetting bistable 64/2 via gate 63/11 and inverter 63/8, Gate 63/11 forms an AND gate so that the manual RESET push-button can also reset bistable 64/12.

3.6.6. The manual (stop) gating on the Input C line follows the same principle as on Input B.

3.7. **Control Logic-Sequence of Operation(Fig 1 G)**

3.7.1. The following paragraphs outline the sequence of operation with stored display selected and the HOLD and RESET push-buttons not selected. Non-stored display operation and manual HOLD and RESET operation are discussed under separate headings.

3.7.2. As previously mentioned under the mode descriptions, the gate open signal is applied to either bistable 60/6 (Frequency and Average Period Modes) or 60/7 (Time, Count, Period and Pulse width Modes). Both outputs affect the output of gate 59/8 which in turn, affects the remainder of the control logic during the 'gate-open' period. The state of control logic outputs during the gate open period is as follows:

(a) gate 59/8 is at logic 0,

(b) inverter 63/3 is at logic 1,

(c) 'stop' bistable Q62/12 at logic 0,

(d) 'reset' bistable Q 48/12 at logic 0,

(e) 'transfer' bistable Q48/9 at logic 0,

(f) gate 51/12 at logic 1,

(g) inverter 41/8 at logic 0,

(h) gate 54/3 at logic 1,

(j) gates 54/6 and 54/11 at logic 0,

(k) gate 59/6 at logic 1,

(m) gates 52/8, 52/6 and inverter 34/12 at logic 0,

(n) gate 51/6 at logic 1.

3.7.3. With gate 59/8 at logic 0, transistor TR20 is cut off and the GATE OPEN indicator lights-up. At the end of the 'gate-open' period, the output of gate 59/8 changes to logic 1, the GATE OPEN indicator is extinguished, and the state of the control logic output points changes as follows:

(a) output of inverter 63/3 drops to logic 0,

(b) Q output of 'stop' bistable 62/12 changes to logic 1,

(c) output of gate 51/12 changes to logic 0,

(d) output of inverter 41/8 changes to logic 1,

(e) output of gate 54/3 drops to logic 0,

(f) output of gates 54/6 and 54/11 changes to logic 1.

Gates 54/6 and 54/11 at logic 1, reset the divider decades to zero.

3.7.4. At this point the control logic employs the 2MHz, $\overline{2MHz}$, 1MHz and $\overline{1MHz}$ outputs of the internal clock oscillator to continue the sequence. With the logic in the state listed above, the next negative-going transient of the $\overline{1MHz}$ output from inverter IC34/8 clocks 'transfer' bistable 48/9, setting its Q output to logic 1. This is applied to gate 59/6 which also gates together the 2MHz output from IC35 (on pin 2) and the $\overline{1MHz}$ output of inverter 34/8. This causes the output of gate 59/6 to drop to logic 0, returning to logic 1 at the next $\overline{1MHz}$ negative-going transient at pin 1. The inverse of this pulse appears at the output of gates 52/8, 52/6 and inverter 34/12, this being the transfer pulse. This is fed to the stores on the main counter circuit as strobe pulses 1 and 2, transferring the counter value reached during the gate-open period to the counter store, and thus to the indicator tubes.

3.7.5. The negative-going trailing edge of the transfer pulse, at the output of inverter 34/12 clocks the 'reset' bistable 48/12, causing $\overline{Q}$ 48/12 to change to logic 0. This is the start of the 'reset' period, and causes the outputs of gate 51/12 and inverter 41/8 to change state to logic 1 and logic 0 respectively. This level change sets the divider decades to 9.

3.7.6. Q48/12 applies a logic 1 to gate 51/6 which also gates in the $\overline{2MHz}$ clock and the $\overline{1MHz}$ clock pulse trains. When all input pins are at logic 1, the output of gate 51/6 drops to logic 0 and this level is applied to the 'reset' input pin (2) of the 'stop' bistable 62/12. This causes $\overline{Q}$62/12 to change to logic 0 removing the stop signal from the channel select gates on the input amplifier board,thus enabling the counter for the next measurement sequence. The output of gate 54/3 changes to logic 1 causing the outputs of gates 54/6 and 54/11 to change to logic 0, ready for the next gate open period. Setting the divider decades to 0 earlier on in the sequence and then setting them to 9 at this time, enables the instrument to be immediately ready for the next measurement sequence.

3.7.7. **Non-STORED Display Selected.** With the STORED push-button released, a logic 1 is applied to pin 5 of gate 43/6. Pin 4 of this gate is also at logic 1 during the gate open period. A logic 0 is therefore applied to pin 9 of gate 52/8 and Pin 5 of gate 52/6, the outputs of which are at logic 1 during the gate open period, thus enabling the store. The counter value is therefore shown by the numerical indicator tubes as the count value builds up. At the end of the measurement, the gate closed period starts and the output of gate 43/6 changes to logic 1. The outputs of gates 52/8 and 52/6 go to logic 0, inhibiting the store thus holding the reading, until the start of the next measurement.

3.7.8. **Manual HOLD and RESET Selected.** With the HOLD push-button depressed, pin 8 of gate 39/8 is at logic 1, so that the J input of bistable 48/12 is at logic 0 and the bistable is inhibited. This means that when the transfer pulse occurs, its trailing edge has no effect on this bistable (see Para. 3.7.4.) and no reset period occurs. Gate 59/6 continues generating transfer pulses, but these also have no effect. However, when the RESET push-button is depressed, (or an external reset signal is applied) the J pin of bistable 48/12 changes to logic 1 and the instrument is reset on the occurrence of the next transfer pulse.

3.8. Variable Display Time Circuit (all modes except Time and Count).

3.8.1. The variable display time circuit consists of content current source TR18 (with R110, R81, RV3, R80, C18 and R11) operating with monostable IC42 and Schmitt trigger TR14 (CA3046/1). The following description is considered in three circuit conditions.

(a) DISPLAY TIME set in, HOLD not selected.

(b) DISPLAY TIME at OFF, HOLD not selected.

(c) HOLD selected.

3.8.2. **DISPLAY TIME set in, HOLD not selected.** With a display time set in by RV3, TR15 is conducting and TR14/14 is off. During the gate open period capacitor C18 is discharged. When the gate closes, a logic 0 is applied to monostable clock input IC42. This fires the monostable, which, during its set state (logic 1) ensures that C18 is fully discharged by switching TR19 on via gate IC40/3. When the monostable output returns to the stable state, TR19 is switched-off, and capacitor C18 is allowed to charge. When the voltage across R11/C18 reaches the threshold voltage of the Schmitt trigger (approx. 2.3V), the Schmitt trigger output changes to logic 1, and is applied to pin J of the reset bistable IC4812/via IC39/8 and IC43/8. Up to this time, the reset bistable could not produce a reset pulse, so that the display remained activated for this period. With a logic 1 applied to pin J of IC48, the bistable is enabled, and a reset pulse is generated at the next transfer pulse.

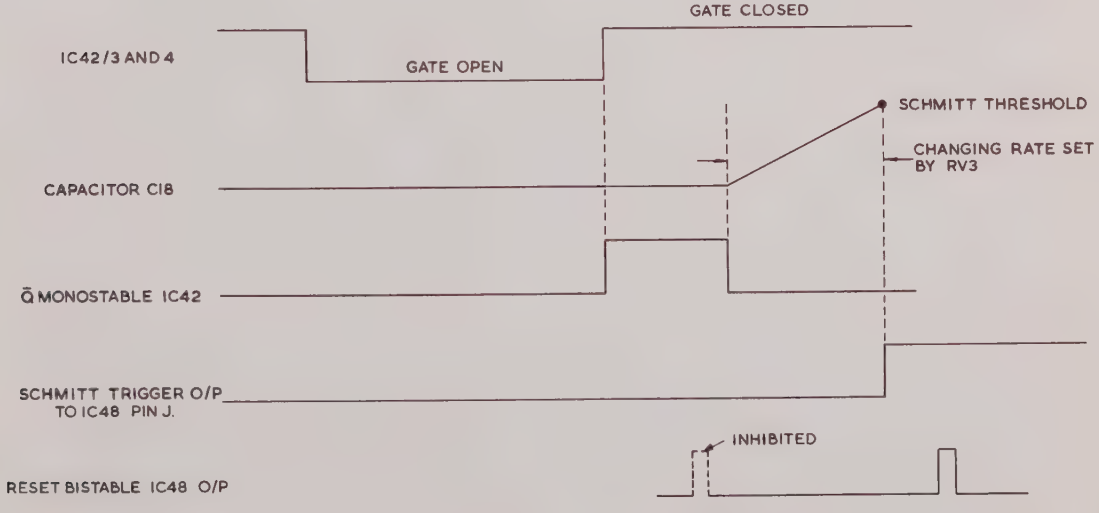


FIG. 4.2. VARIABLE DISPLAY TIMING DIAGRAM

3.8.3. When the gate closes, the output of the schmitt trigger changes to logic 0 at this time. This is ensured by the action of the firing circuit TR14/11, which accepts the gate open/gate closed waveform as its input. This circuit is required, as the capacitor discharge time is too slow.

3.8.4. **DISPLAY TIME at OFF, HOLD not selected.** In this condition, the amount of current flowing through R11 ensures that the voltage applied to TR14, pin 6 (CA3046) is always at the Schmitt trigger threshold level. The output of the Schmitt trigger is, therefore, held at logic 1, so that the reset bistable is permanently enabled. This means that a reset pulse is generated after every transfer time.

3.8.5. **HOLD selected.** In the HOLD mode, the output of the Schmitt trigger has no effect on pin J of the reset bistable IC48, as gate IC 39/8 is held at logic 1 by the HOLD push-button. Pin J of IC48 is therefore clamped at logic 0. A reset pulse can, therefore, only be produced by the usual manual or external method via gate IC43/8. If HOLD is selected whent he instrument is switched-on, the automatic reset circuit D8/C23 still operates.

3.9. **Variable Delay Time Circuit (Time and Count modes only).**

3.9.1. The variable delay time circuit consists of constant current source TR17 (with R77, RV3, R110, R80, R78, C17 and TR16). C17 is the timing capacitor. In the time and count modes, the reset bistable IC48 is permanently enabled. The gate-open/gate-closed waveform is initiated by bistable IC64/12, which in turn, triggers gate-open bistable IC60/7.

3.9.2. The purpose of the delay time is to stop the gate being closed, once it has been opened for a set period of time. Subsequent false stop pulses (due to contact bounce, for instance, from external devices) are inhibited. These, would otherwise, cause the gate to close again, giving a false display value.

3.9.3. Consider the instrument set the the B-B gating mode (see fig. 4.3.). During the gate-closed period, the output of bistable QIC64/12 is at logic 0, so that transistor TR16, ensures that C17 is fully discharged. Bistables QIC45/9 and QIC45/12 charge to logic 0, when the pulse on the output of gate IC51/6 occurs.

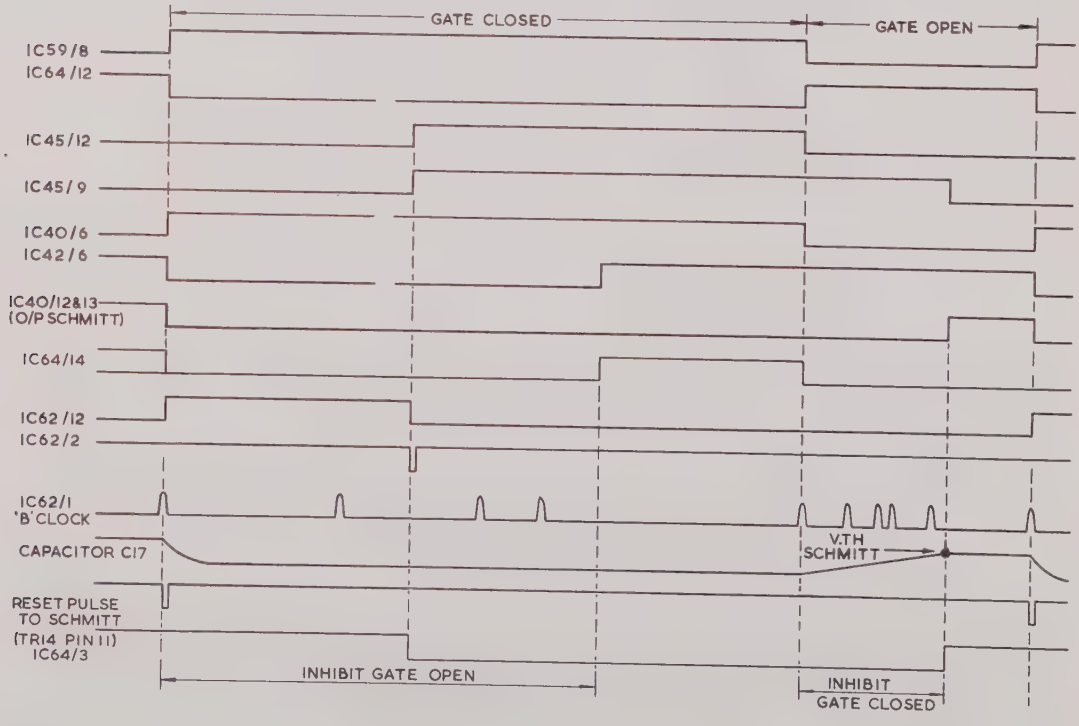


FIG. 4.3 TIMING DIAGRAM OF B–B GATING MODE WITH VARIABLE DELAY

When a B input start signal clocks bistable QIC64/12, its ouput charges to logic 1, switching off TR16. Capacitor C17 starts to charge, the time taken being dependent upon the setting of RV3. During this time, the Schmitt trigger output (CA 3046) pin 1 is at logic 0, so that a logic 1 is applied to bistable IC45/9, pin 6. Bistable IC45/12 is reset to logic 0 (Q64/12 is on logic 0 as the gate open period is in operation).

3.9.4. When capacitor C17 reaches the threshold voltage of the Schmitt trigger, its output changes to logic 1, so that a logic 0 is applied via IC40/11 to the reset pin of IC45/9. The Q output of this bistable changes to logic 0. As the K input of bistable IC64/12 is at logic 1, IC64/12 is enabled, so that the gate can close when the next B input stop pulse occurs.

3.9.5. From the above description, it can be seen that bistable IC45/12 ensures that the gate-open bistable IC64/12 dosn't change state during the 'gate-closed' display time. Bistable IC48/9 ensures that bistable IC64/12 is inhibited during the variable delay time.

3.10. Units Display.

3.10.1. The units display is controlled by gates on IC1, IC2, IC3, IC5, IC6. These gates apply a code to IC4 and IC7. These in turn, drive the unit display tubes V1 and V2. The codes produced by the gates differ, depending upon the range code applied and the operational mode in use. A truth table for each mode and range is given on fig. 1A Display and Logic Board,circuit diagram.

3.10.2 The code is applied to IC4 and the output illuminates the decimal point in the appropriate numerical indicator tube. The 'D' input to IC4 drives indicator tube V1 to illuminate the appropriate unit, Hz or S.

3.10.3. A code formed on the input pins of IC7 produces an output on one of its four output pins. This output drives indicator tube V2 to illuminate the appropriate multiplcation factor, M, K, m or μ. At certain position permutations of the range and mode switches, transistor TR3 conducts (a logic 1 is applied to the base) inhibiting V2. These positions can be deduced by reference to the truth table on fig. 1A Display and Logic Board,circuit diagram.

3.11 Counter Circuit

3.11.1 The counter circuit is distributed over two p.c. boards as follows:

(a) Input Amplifier Board (fig. 3.) This contains the first (units) decade (1248) and the first stage (10) of the second decade.

(b) Display and Logic Board (fig. 1A). This board contains:

(i) last three stages of the second decade (IC12) and the remaining counter decades (IC's 15, 18, 21, 24, 27, 30) eight stores (IC's 7, 11, 14, 17, 20, 23, 26, 29) eight decoders and eight numerical indicator tubes (V3 to V10).

(ii) overrange bistable (IC32/9) fed from the eighth counter decade on the display and logic board.

3.11.2. On the input amplifier board, the first decade of the counter is split between the first bistable (1) and the remaining three bistables (2, 4 and 8). This first bistable is selected from one of two bistables, IC3 or IC4, depending upon which operating mode has been selected. This is shown in the table below:

Mode	Bistable Selected	Triggered By
Frequency	IC3	Incoming signal
Period/Pulsewidth	IC4	Internal clock
Count (Range 1)	IC3	Incoming signal
Count(Range 2 - 6)	IC4	Internal clock
Time	IC4	Internal clock
Average Period	IC4	Internal clock

3.11.3 Each bistable is connected to the remaining stages of the 1st decade by a latch and two channel selecting gates. A logic 1 (0V) applied to the clock input of each latch enables it and the output of the first selected bistable is passed through to the channel select gates on IC8. These are controlled by the channel select input applied to R53; a logic 0 (-5.2V) applied to a gate on IC6 enables it.

4. BCD FAN OUT AND PROGRAMME UNIT SM 248

4.1. This unit, which is fitted to the '/B' versions of the SM 202 only, is an optional fitting for the basic version and can also be supplied in kit form. It consists of p.c. board wired to a 50-way socket and an 18-way plug. The board is plugged into an edge connector (SK2) on the display and logic board.

4.2. **8-Decades of BCD and Overrange.** These levels are taken from the outputs of the stores on the display and logic board and are fed via SK2 to buffer gates IC 3 to IC 11. The outputs of these gates are fed to the 50-way PRINTER OUTPUTS socket on the rear panel.

4.3. **Print Command.** The print command pulse is derived from the transfer pulse, by the action of the monostable IC2. During the gate open period, the input A1 line to IC2 is enabled by a logic 1 on pin A2. When the gate closes at board pin 18b, pin 1 of IC 1 goes to logic 1. The negative-going edge of the transfer pulse at IC1/11 output triggers monostable IC2, causing the $\overline{Q}$ output to drop to logic C This triggers the latch IC 1/3 and 6. 1C 2 is then inhibited by a logic 0 on pin A1 (3). Once triggered, the output is independent of further transitions on the inputs and is a function only of the timing components, capacitor C1 and resistor R1. After 7 µs, the $\overline{Q}$ output changes to logic 1. A positive-going 7 µs pulse appears, therefore, at IC1/8; this is the print command.

4.4. **Range Outputs.** The range output code is applied to board pins 22b, 21b and 20b. This is inverted by IC's 16/8, 18/12 and 18/8 and routed to the 50-way Printer Output socket on the rear panel.

4.5. **Mode Outputs.** These levels are derived from the mode switches and are applied to buffer inverters on IC's 12/6, 12/11, 18/4, 18/10 and 16/4. A selected mode is represented by a logic 1 at the relevant pin on the 50-way Printer Output socket on the rear panel.

4.6. **Other Functions.** These are also buffered and inverted before application to the relevant output pins on the 50-way Printer Output socket. These functions are their operative logic states are listed below.

Function	Pin No.	Operative Logic State
Hold	B11	Logic 1
External Clock	C11	Logic 1
Gating Mode	D11	Logic 1 for B-B, Logic 0 for B-C
Store	A12	Logic 1
Totalise	B12	Logic 1
External Programme	C12	Logic 1
0V Reference	A13, C13	——

4.7. **External Programming.** When the EXT PROG push-button is depressed, input NAND gates 12/3, IC14, IC15, IC17, IC19, are enabled (a logic 1 is applied to board pin 25a) and all the front panel push-buttons are disconnected from 0V, disabling all manual functions. The external program functions described in the following paragraphs are therefore enabled.

4.8. **Range Address Inputs.** This is a code applied to pins A1, B1, C1 of the 18-way EXTERNAL PROGRAM INPUTS plug which automatically sets the units display logic (fig. 1A) to position the decimal point correctly and display the assigned measurement unit (kHz, MHz, etc.) The range address code is also applied to the buffer inverters on the BCD board, so that they are available to an external printer.

Range Address	Pin No. C1	B1	A1
	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

4.9. **Mode Address Inputs.** These are applied to the relevant pins of the 18-way EXTERNAL PROGRAM INPUTS plug. A logic 1 input level selects the mode.

4.10. The remaining programmable functions and their operative logic states are listed below:

Function	Pin No.	Operative Logic State
External Reset	A3	Logic 1
Hold	B3	Logic 1
External Clock Address	C3	Logic 1
Gating Mode	D3	Logic 1 for B-B Logic 0 for B-C
Store	A4	Logic 1
Totalise	B4	Logic 1
0V Reference	C4, D4	———

4.11. **The +5V d.c. (Vcc) supply** to the p.c. board is protected by a 250mA fuse FS1, and is further stabilised by Zener diode D (Z) 1. Capacitor C2 protects all circuitry from the effects of transients.

5. POWER SUPPLY

5.1. The power (mains) is fed via the mains input socket, switch SW5 and 200mA fuse FS1 to the primary of mains transformer T1, the tappings of which are linked in series for 230V mains operation, or in parallel for 115V mains operation.

5.2. Six supplies are generated:

(a) +250V unstabilised supply for the numerical indicator tubes, gate-open indicator and overrange indicator.

(b) +12V stabilised supply for the input amplifier board, display and logic board, and active probe supply socket.

(c) -12V Zener stabilised supply for the active probe supply socket.

(d) +5V stabilised supply for the display and logic board, and BCD board.

(e) -5.2V stabilised supply for the input amplifier board and, display and logic board.

(f) +12V (nominal) oven supply, for the crystal oven heaters.

5.3. **+250V Supply.** This is derived from secondary winding W1, rated at 22mA. It is half-wave rectified by diode D1 and fed to pin a on the display and logic board.

5.4. **+12V Supply.** The + 12V supply is derived from secondary winding W2, rated at 150mA. It is full wave rectified by bridge rectifier D4, D5, D6, D8 and stabilised by the integrated circuit regulator IC3.

5.5. **-12V Supply.** This supply is Zener stabilised by D (Z) 9 and fed to the active probe supply socket on the rear panel of the instrument.

5.6. **+5V Supply.** This is full-wave rectified by bridge D2 and stabilised by integrated circuit regulator IC2 controlling series transistor TR1.

5.7. **-5.2V Supply.** The -5.2V supply is derived from winding W4 (rated at 500mA) and is bridge rectified by D7, with stabilisation provided by IC4.

5.8. **+12V Oven Supply.** This is Zener stabilised by D (Z) 2. At switch-on, this supply provides a current of 2.7A (approx.) to heat the crystal oven. Winding W3 is rated at 22mA with the capability of supplying 2.7A for about 3 minutes.

SECTION 5

MAINTENANCE

1. INTRODUCTION

1.1. This section contains maintenance, calibration and service information. Included is information on preventive maintenance, a list of recommended test equipment, and checks and adjustments.

2. PREVENTIVE MAINTENANCE

2.1. Instrument Cover Removal

(a) To remove the top cover, remove the two screws that secure the cover to the instrument, at the rear.

(b) Slide the cover rearwards. To refit the cover, reverse the procedure.

WARNING

115V/230V a.c. and d.c. supply wires are exposed when the top cover is removed. Disconnect the power lead before removing the covers.

2.2. Cleaning

2.2.1. The instrument should be cleaned as often as operating conditions require. Accumulation of dust in the instrument can cause overheating and component breakdown. Dust on components acts as an insulating layer, thus preventing efficient heat dissipation.

2.2.2. Thoroughly clean the inside and outside of the instrument. Remove dust from inaccessible areas with low pressure, compressed air. Use alcohol applied with a brush to remove accumulations of dust or grease from connector contacts and component terminals. Clean the exterior of the instrument and the front panel with a mild detergent mixed with water, applying the solution with a soft, lint-free cloth.

2.3. Visual Inspection

2.3.1 The SM202 should be inspected occasionally for broken connections, loose, broken or frayed wiring, dirty or pitted switch and connector contacts and cracked or broken printed circuit boards. Often, before a failure occurs, a deteriorating component can be located due to obvious discolouration, cracking or warping.

2.3.2. Care must be taken when heat-damaged parts are located. Overheating is usually only a symptom of trouble. For this reason, it is essential to determine the actual cause of overheating before the heat-damaged part is renewed, otherwise the damage may be repeated.

3 REPAIR AND RENEWAL OF PARTS

3.1 Repair and renewal of electrical and mechanical parts must be carried out with caution. Printed circuit component boards can become warped, cracked or burnt from excessive heat or mechanical stress. The following repair techniques are suggested to avoid inadvertent destruction or degradation of parts and assemblies.

3.2 Use ordinary 60/40 solder and a 35W or 40W pencil type soldering from on the circuit board. The tip of the iron should be clean and properly tinned for best heat transfer to the solder joint. A higher wattage soldering iron may separate the circuit from the base material. To de-solder components, use a commercial solder sipper.

3.3. Always renew a component with its exact duplicate as specified in the parts list.

4. CHECKS AND ADJUSTMENTS

4.1. Test Equipment

(a) V.H.F. signal generator, frequency range up to 150MHz sinewave, at 2.5V (General Radio, Type 13363 with regulated supply 1267/B, or similar). 50 Ω termination.

(b) Frequency standard, with 100kHz and 90MHz outputs (Jacel Frequency Meter 331, or similar).

(c) Sinewave oscillator, frequency range up to 1MHz at up to 5Vp-p (Levell Oscillator Series IG66, or similar).

(d) Sinewave/squarewave oscillator , frequency range up to 150kHz at up to 2.5pk (Levell Oscillator TG150D or similar).

(e) Dual beam oscilloscope, bandwidth up to 150MHz (SE Laboratories SM112 Oscilloscope fitted with SM599 Y–Amplifier, or similar) x1 and x10 probes.

(f) Millivoltmeter (Farnell TM6 or similar).

(g) DC supply up to ± 2V d.c. (Weir 'Minireg' or similar).

(h) Multimeter (Avometer model 8 or similar).

(j) Mains variac.

4.2. Power Supply Checks

(a) Disconnect the power supply leads from the main board ensuring that they cannot make contact elsewhere.

(b) Connect the unit mains lead to a variac, set at 30V r.m.s.

(c) Switch on the SM202 and check that the voltage across all electrolytic capacitors is of the correct polarity.

(d) Raise the variac voltage of 230V r.m.s. and using the Avometer Model 8, check the supply rail voltages.

Supply Rail	Min.	Max.
–5.2V	– 4.9V	–5.5V
+12.0V	+ 11.4V	+12.6V
+5.0V	+ 4.75V	+5.25V
–12.0V	–11.4V	–12.6V
Indicator Supply	+88V	+ 98V

(e) Switch off the SM202, reconnect the power supply leads.

(f) Switch off the SM202 and check that the supply rail voltages fall within the limits given in para. (d).

(g) *Ripple Checks.* Using the Oscilloscope SM112 with an x1 probe and a short earth lead connected to the 0V rail of the SM202 (pin bw, or nearest convenient point), check the ripple voltages on each rail, to be within the limits stated below.

Supply Rail	Test Point	Ripple Limit (pk-pk)
– 5.2V	bh	Not greater than 8 mV
+ 12.0V	bg	Not greater than 20mV
+ 5.0V	ah	Not greater than 50mV
– 12.0V		

Set the Variac at 195V r.m.s. and repeat the checks in steps (d) and (g).

(h) Check that the probe supplies are correct at the Active Probe Supply socket as follows:-

4.3. Channel A Amplifier

NOTE: Ensure that, before carrying-out this check, the power supplies check-out correctly as in Para. 4.2.

(a) Connect the x10 probe of the oscilloscope to the high output pin bu and check that when the LEVEL control is moved from end-to-end, the indicated voltage varies between 0V anticlockwise to –4V clockwise.

(b) Connect a 1kHz sinewave signal to the input of the assembly and select the 10 mV SENSITIVITY position. Adjust the amplitude of the input signal to give an output signal of 150mV peak-to-peak. This should be 10 mV peak-to-peak, ± 5%.

(c) Switch to the 100 mV SENSITIVITY position and check that the input amplitude, to achieve an output of 150mV peak-to-peak, is 100mV peak-to-peak, ± 5%.

(d) Switch to the 1V SENSITIVITY position and check that the input amplitude, to achieve an output of 150mV peak-to-peak, is 1V peak-to-peak, ± 5%.

(e) Switch to the 10V SENSITIVITY position and check that the input amplitude, to achieve an output of 75 mV peak-to-peak, is 5V peak-to-peak.

(f) Change the input signal from 1kHz to 1MHz using the test sinewave oscillator.

(g) Repeat the checks carried out in steps (b) to (e), ensuring that the inputs necessary to give 150 mV and 75 mV outputs are as stated, but to the following tolerances;

Range	Tolerance
10mV	± 10%
100mV	± 10%
1V	– 5% to +50%
10V	+ 5% to –50%

4.4. Decimal Point Operation.

NOTE: The indicator tubes for this check are numbered 1 to 10 from left to right. The range push buttons are numbered 1 to 7 from left to right.

(a) Switch on the SM202 and select in turn FREQUENCY, PERIOD or TIME, AVERAGE PERIOD, and COUNT. For each mode of operation, check the decimal point position and the units indicated with the following table.

MODE	RANGE	TUBE DECIMAL POINT								UNITS	
		1	2	3	4	5	6	7	8	9	10
Frequency	1								●	M	Hz
	2							●		M	Hz
	3						●			M	Hz
	4					●				M	Hz
	5							●		K	Hz
	6						●			K	Hz
	7					●				K	Hz
Period or Time	1					●				M	S
	2						●			M	S
	3							●		M	S
	4								●	M	S
	5						●				S
	6							●			S
	7								●		S
Average Period	1								●	μ	S
	2							●		μ	S
	3						●			μ	S
	4					●				μ	S
	5				●					μ	S
	6			●						μ	S
	7		●							μ	S
Count	1 to 7	No decimal points illuminated. No indicated units.									

4.5. Automatic Reset.

(a) Switch off the SM202. Ensure that the EXT CLOCK and EXT PROG buttons are released.

(b) Switch the SM202 and check that all zeros are displayed and that the OVER-RANGE lamp is not illuminated.

4.6. External Programming, Reset Inhibit Check

(a) Check that when the EXT PROG button is pressed, the EXT PROG neon illuminates and that by depressing the RESET button, the display is not reset to zero. Release the EXT PROG button.

4.7. TIME Mode

(a) Select TIME Mode, Internal Clock, B-B gating mode and adjust the DELAY TIME control fully anticlockwise.

(b) Check that with successive operations of the B channel polarity switch to the spring loaded MANUAL position, the gate opens and closes.

(c) Check that by operating the C Channel polarity switch in a similar manner, it has no affect on the gate light.

(d) Operate the B channel switch to open the gate and check that by depressing the RESET button, the gate lamp extinguishes and the display resets to zero.

(e) Check, that the display counts correctly, by observing that each indicator tube displays 0 to 9 correctly. This can be done by selecting a range such that, the tube being observed counts slowly enough, to be certain each figure is illuminated in turn.

(f) Check that as tube 1 (extreme left) changes from 9 to 0, the OVER-RANGE light is illuminated. Check also that, as this stage is reached on subsequent occasions, it remains illuminated.

(g) Select the B-C mode and check that with successive operations of the B channel polarity switch to the spring loaded MANUAL position, the GATE OPEN light illuminates and remains so throughout all subsequent operations of the B switch.

(h) Check that by operating the C Channel polarity switch to the spring loaded MANUAL position, the GATE OPEN light is extinguished and remains so throughout all subsequent operations of the C switch.

(j) Repeat these operations for the B and C switches a few times and at one stage, when the gate light is illuminated, check that operating the RESET button, once, closes the gate, (extinguishes the light).

(k) Select the B-B Mode. Select HOLD with the gate light extinguished. Check that operating the B switch to the MANUAL position opens the gate on the first operation, closes it on the second operation, and has no further action on subsequent operations.

(m) Release HOLD, open the gate, and by use of the B switch, select HOLD. Check that by operating the B switch once more, the gate closes and subsequent operations have no effect.

(n) Operate RESET once and check that one further cycle only, of opening and closing the gate, can be achieved.

(p) Release HOLD. Check for each tube, by using the most convenient range, that the count obtained is held when the gate is closed and returns to zero when the gate is reopened.

(q) Select STORED and check that the display is up-dated correctly, when the gate is successively opened and closed.

(r) Select TOTAL, and release STORED. Using the most convenient range for viewing, check that the readings are added when the gate is successively opened and closed, and that no RESET occurs.

(s) Press the RESET button and note that the display resets to zero.

(t) Select STORED and repeat step 4.6. (a) noting that correct up-dating

(u) Select TIME Mode, B-B gating mode. Non-Stored display, Range 1 and a B SENSITIVITY position of 0.1 V. Adjust the B trigger LEVEL control backwards and forwards over a limited range gradually covering the whole span of the control. Note the position where the gate light goes on and off and the unit operates. This position should be the approximate centre of the control range.

(v) Apply a +2V signal from the test d.c. supply to the B channel input. Repeat the backwards and forward movement of the B trigger LEVEL control noting the position where the gate light goes on and off; this should be some 110^{O} clockwise from the point established in step (u) above.

(w) Apply a -2V signal from the test d.c. supply to the B channel input. Repeat the operation described in step (v) above, noting the position where the gate light goes on and off; this should be some 110^{O} anticlockwise from the point established in step (u) above.

(x) Select B-C gating. Non-Stored display, Range 1 and a C SENSITIVITY position of 0.1V. Set the C polarity switch to -VE, and open the gate by manual operation of the B channel switch. Rotate the C trigger LEVEL control clockwise, noting the position where the gate light extinguishes. Repeat this operation.

NOTE: It will be found necessary to turn the C trigger LEVEL control fully anti-clockwise before reopening the gate with the B manual switch.

(y) Apply a +2V signal from the test d.c. supply to the C Channel input and repeat the operations described in step (x) above; the trigger point should move 110^{O} clockwise from the point established in step (x) above.

(z) Select the +VE polarity of the C manual switch and apply a +2V signal from the test d.c. supply to the Channel C input. Repeat the operation of step (x) above, but adjusting the C trigger LEVEL control anti-clockwise to close the gate. Note that the trigger point occurs some 110^{O} anti-clockwise from the point established in step (x) above.

4.8. COUNT Mode(Range 1 Only)

(a) Select COUNT Mode, Non-Stored display, Range 1 (extreme left) and DC coupling. Operate the B switch to open the gate and successively swing Channel A LEVEL control throughout its range. Each time the control knob passes through the central position, the display should increase by one unit.

(b) Select the 10 mV position on Channel A SENSITIVITY switch and apply a 25 mV peak-to-peak signal of 100 MHz sinewave, terminated in 50 ohms, from the v.h.f. signal generating to pin A. Note that correct counting is obtained with the LEVEL control set approximately halfway between the control knob limits.

(c) Disconnect the signal from input A and select 0.1V on the input A SENSITIVITY switch. Apply a +2V signal from the test d.c. supply to input A. Swing the LEVEL control and note that the trigger point moves from centre 110^{o} towards the positive end of the control. Using a -2V signal applied to input A, note that the trigger point moves 110^{o} from centre to the negative end of the control.

(d) Select AC coupling on Channel A and check that the trigger point now returns to the central position of the control.

4.9. FREQUENCY Mode.

(a) Select FREQUENCY mode, STORED display, Range 1 (extreme left) 10 mV position of the input SENSITIVITY switch and set the DISPLAY TIME control fully anti-clockwise. Apply a 25 mV peak-to-peak signal of 100 MHz sinewave, terminated in 50 ohm from the v.h.f. signal Generator to input A. Check that by using the LEVEL control, a stable correct reading can be obtained.

(b) Select, in turn, ranges 2 to 7 noting the consistency of readings.

(c) Repeat steps (a) and (b) above for different settings of the DISPLAY TIME control.

(d) Select Range 4. Adjust the amplitude of the input signal, using the test millivoltmeter, to 8 mV r.m.s. and note the maximum frequency where stable repeatable counts are obtained.

(e) Re-adjust the amplitude to 50 mV r.m.s. and, again, note the maximum frequency where stable repeatable counts are obtained.

(f) Select the 100 mV position of Channel A SENSITIVITY switch. Set the input amplitude to 80mV r.m.s. on the millivoltmeter and note the maximum frequency where stable repeatable counts are obtained.

(g) Re-adjust the amplitude to 100 mV r.m.s. and, again, note the maximum frequency where stable repeatable counts are obtained.

(h) Check that the noted maximum frequencies remain the same for the AC and DC positions of Channel A coupling switch.

4.10. Display Time.

(a) Using the oscilloscope and a x10 probe, observe the signal at pin 8 of I.C.59, the 0 level indicated being the gate open time and the 1 level being the display time duration. Ensure that the display time covers the range 3 μs to 3.0 secs (approx.)

4.11. Timebase Calibration

CAUTION

This check must only be carried out after the unit has been running for at least 30 minutes.

(a) Select FREQUENCY mode, STORED display, Range 4. Using the 90 MHz output signal from the frequency standard applied to Channel A input, adjust the crystal oscillator trimming capacitor for a displayed reading of 90,0000 MHz.

(b) Select Range 6 and adjust the crystal oscillator trimming capacitor for a displayed reading of 90,000,000 kHz flickering by ± 1 bit.

(c) Select Range 5. The displayed reading should be 90,000,00 kHz ± 1 bit. This checks that the constant gate time error is less than 11 ns.

4.12. AVERAGE PERIOD Mode

(a) Select AVERAGE PERIOD mode, STORED display, Range 3, and the 10 mV position on Channel A SENSITIVITY switch. Apply a 100 kHz signal from the Frequency Standard to input A. Check that the display reads 00010.000 μs ±1 bit.

(b) Select range 7. Check that the OVER-RANGE light illuminates and the display reads 0.0000000 μs ±1 bit.

(c) Disconnect the input. Select range 2 and using Channel A LEVEL control, open the gate. Check that by operating the RESET button, once, the gate closes and resets the display to zero.

4.13. PERIOD Mode.

(a) Select PERIOD mode, STORED display, Range 1, AC coupling, 10 mV position on Channel A SENSITIVITY switch and the PERIOD position of the PERIOD/PULSEWIDTH switch. Apply a 500 mV peak-to-peak sinewave of 100 Hz from the sinewave/squarewave test oscillator to input A to give a display of approximately 0010.0000 ms. Adjust the frequency of the oscillator to give a convenient beat frequency with the internal ripple of say,1Hz. Check that the observed variations on the display, due to the beat, are less than 100 bits total.

(b) Change the frequency of the input signal to 10 Hz. Select range 3 and check that a stable display can be obtained with a variation on the display due to the beat, of less than 100 bits total.

(c) Change the oscillator sginal to 25 mV peak-to-peak, squarewave of 1 kHz, and connect the x 10 probe of the oscilloscope to pin 8 of I.C.59, also observing simultaneously the input waveform on the other oscilloscope channel. Trigger the oscilloscope from the I.C. signal. The waveforms shown in fig. 6.1. are displayed for the different positions of the PERIOD/ PULSEWIDTH switch.

(d) Change the oscillator signal to 25 mV peak-to-peak 10 Hz squarewave. Check that the instrument operates correctly by producing the waveforms as indicated. Adjust the LEVEL control and check that the output waveform moves in-phase with the input.

4.14. B and C Amplifiers.

(a) Select TIME mode, B—B gating mode, non-stored display and Range 1. Connect the x10 probe with the oscilloscope to pin 6 of I C.33. Check, by manually operating the B LEVEL control that the gate opens and closes approximately half way between the extreme limits of the LEVEL control knob.

(b) Repeat step (a) above for all SENSITIVITY positions of Channel B, checking that the trigger point remains in approximately the same position.

(c) Select the 0.1V SENSITIVITY position of Channel B and apply a 250 mV peak-to-peak, 10 MHz, sinewave signal to the B input. Observe the waveform on the osciloscccope and check that it is a clean, stable, squarewave and that the mark:space ratio changes with the setting up of the LEVEL control.

(d) Select the 1V SENSITIVITY position of Channel B and increase the signal amplitude to 2.5V peak-to-peak. Repeat observations as for (c).

(e) Select the 0.1V SENSITIVITY position of Channel B and apply a 250 mV peak-to-peak sinewave, noting the maximum frequency in MHz, where stable operation occurs.

(f) Select the 1V SENSITIVITY position of Channel B and apply a 2.5V peak-to-peak sinewave, noting the maximum frequency in MHz, where stable operation occurs.

(g) Select the 10V SENSITIVITY position of Channel B and apply a peak-to-peak sinewave, noting the frequency in MHz where stable operation occurs.

(h) Select B—C gating mode. Connect the x10 probe with the oscilloscope to pin 8 of I C.33. Open the gate by operating the B switch to the MANUAL position. Check that the trigger point of the C amplifier is approximately half way between the extreme limits of the LEVEL control knob, and remains so for the various SENSITIVITY positions of Channel C input.

NOTE: Should the trigger point be at a position other than the approximate mid-point on either the B or C channel LEVEL controls, then the appropriate A.O.T. resistors require changing (for Channel B, R.40 or Channel C, R42.)

(j) B Channel L.F. Check. Connect the x10 probe of the oscilloscope to pin 5 of TR7 and apply a 1kHz sinewave signal to the B input. Adjust the input amplitude to give an indicated signal of 50 mV peak-to-peak on pin 5, TR7, with the SENSITIVITY switch on 0.1V. Check that the input is 50 mV p-p, ± 10%. Select 1.0V on the SENSITIVITY switch and check that the input signal has to be raised to 500 mV ± 10% to obtain 50 mV peak-to-peak indication.

Switch to 10.0V on the SENSITIVITY switch and check that the input signal has to be raised to 5V ± 10% to obtain 50 mV peak-to-peak indication.

(k) ***B Channel H.F. check.*** Increase the input frequency to 1 MHz and repeat the checks for the various SENSITIVITY positions as indicated in step (j) above, noting that the input necessary to obtain 50 mV peak-to-peak is as stated, but to tolerances of +0% to -50%.

(m) ***C Channel L.F. check.*** Connect the signal generator set at 1 kHz sinewave to input C and repeat the checks for SENSITIVITY positions as indicated for L.F. and H.F. signals in (j) and (k) respectively, using the x10 probe on TR8, Pin 5.

4.15. Gating Mode.

(a) Select TIME mode, STORED display, Range 1 and set the variable time delay to minimum (fully anticlockwise). Connect the two x10 probes of the oscilloscope to pin 8 of I.C. 59 and pin 8 of I.C.33, oscilloscope channels 1 and 2 respectively. Apply a 10 MHz sinewave signal of 250 mV peak-to-peak simultaneously to pin B and C. Set the SENSITIVITY switches of Channels B and C to the 0.1V positions. Trigger the oscilloscope on Channel 1, the waveforms shown in fig. 6.2 should be observed.

(b) With the input signal set as in step (a) above, the display should indicate 00000000 flashing 1 bit. Slowly, turn the variable delay control clockwise and check that the display reading, after remaining the same, increases, for $30^{0}_{,}$ gradually to approximately 60 ns with the control fully clockwise. The jitter should be less than 0.5% of the total reading.

(c) Repeat the operation described in step (a) above with an input signal of 10 Hz and check the waveforms.

4.16. External Clock.

(a) Select TIME Mode, Non-Stored, Range 1 and B—C Mode. Open the gate by operating the B polarity switch to manual; the instrument should count. Select EXT CLOCK. The unit should stop counting and by operating the B switch to MANUAL, the gate should close. Check the instrument operates as for B—B gating mode and that it is not affected by the C Channel switch.

(b) Using a short length of coaxial cable terminated with B.N.C. plugs, connect the 1 MHz output on the rear panel to input C. Check that by using the B switch to open and close the gate, the instrument counts.

4.17. 1 MHz Clock Output.

(a) Connect the x10 probe of the oscilloscope to the 1MHz output and check that the signal is 1 MHz 0V to +5V squarewave and is free from ringing and reflection.

(b) Select FREQUENCY mode, STORED display, Range 1 and the A input SENSITIVITY switch to 1V position. Connect the 1 MHz output to Channel A input and adjust the LEVEL control for a period of 0000001.0 MHz.

(c) Select AVERAGE PERIOD mode and the reading should be 0000.0010 ms.

(d) Select PERIOD mode and the reading should be 0000.0010 ns with the PERIOD/PULSEWIDTH switch on + or — PERIOD, and 0000.0005 ns with the PERIOD/PULSEWIDTH switch on + or — PULSE. For the +ve and —ve polarities, the LEVEL control must be set for the appropriate polarity.

(e) Remove the signal from Input A and apply it to Input B. Select TIME mode, B—B gating mode and Range 1, the display should indicate 0000.0010 ms.

NOTE: It may be necessary to adjust the LEVEL control for each mode selected.

4.18. COUNT Mode (Ranges 2 to 7)

(a) Select COUNT mode, STORED display, and B—B gating mode. Apply a 500 Hz sinewave signal of 1V peak-to-peak to input B. Apply, to input A on the 1V SENSITIVITY position, the 1 MHz signal from the rear of the unit. Check that the display indicates 00002000.

(b) Select Range 2. The displayed reading of paragraph (a) should now be divided by 10.

4.19 Z Modulation.

(a) Connect the Z Modulation output of the unit to the Z Modulation input of the oscilloscope and apply a 1 MHz sinewave signal from the sinewave TG200 oscillator to the A Input of the SM202, and to Channel 1 of the oscilloscope. Adjust the brilliance of the oscilloscope, commensurate with optimum definition of the trace. The bright-up should be as indicated in the fig. 6.3.

(b) Vary the trigger point by adjusting the A channel LEVEL control on all ranges of the SENSITIVITY switch, observing the waveform.

TABLE 6.4 POWER SUPPLY (Refer to the circuit diagram)

REF	SEL PART NO	MANUFACTURER/DESCRIPTION			
		CAPACITORS (µF)	Value	Tol ± %	Rating
C1	CS 31172	Mullard, 106 15103	10,000	+50,-10	16 V
C2	CS 30176	Mullard, 426AR/E10	10	+50,-10	16 V
C3	CS 31169	Erie,21104/100/0471/0A/0400	470		
C4	As C3				
C5	CS 31168	Erie,21106/100/0222/0A/0160	2,200		16 V
C6	As C2				
C7	CS 30991	I.T.T. Tag 10/16	10	+50,-20	16 V
		DIODES			
D1	BS 2522	Mullard, BYX10			
D2	BS 3057	Motorola,MDA 970A-1			
D3	-				
D4	BS 2365	Motorola,MDA 920A-2			
D5	As D4				
D6	-				
D7	As D4				
D(Z) 10	BS 3110	Motorola, 1N 4728A			
		INTEGRATED CIRCUITS & TRANSISTORS			
IC1	BS 3055	S.G.S.Fairchild,L005			
IC3	BS 3056	S.G.S.Fairchild,L036			
IC4	As IC2				
TR1	BS 2845	Mullard, BSX21			
		RESISTORS (Ω)	Value	Tol ± %	Rating
R1	DS 34000	Mullard, CR25	22	5	¼ W
R3	DS 34320	Welwyn, W21	56	5	2.5 W
R4	DS 34321	Welwyn, W21	82	5	2.5 W
		MISCELLANEOUS			
FS	RS 23113	Fuse Link,250mA,Beswick,TDC123			
	RS 23064	Fuse Holder,Britempex FEP704M/70G			
	AS 0450	Plug,Greenpar BN1/5			
SKT 1	AS 1398	Socket,3 pin,fixed,Electro Methods SM35-N			
SW1	QS 22230	Switch,mains,Painton, 22/10/0201/00			
T1	D 3632	Transformer mains,Ripley,S.E.L. D5/576			
	ES 8377	Transformer, 5/358,Buckingham Electronic			
	GS 11167	Toroid, FX3007,Mullard,240 V			

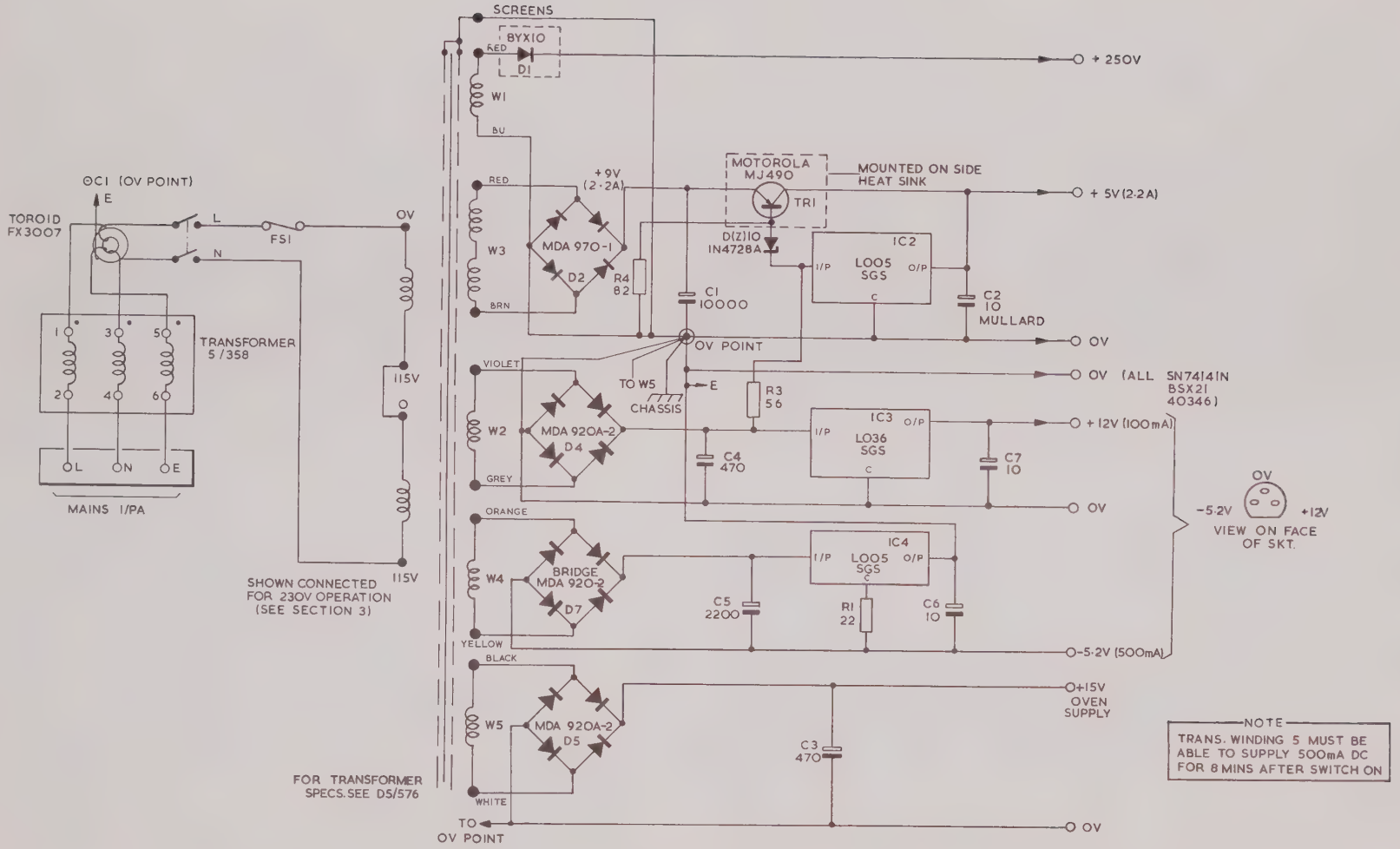


FIG 6. POWER SUPPLY – CIRCUIT DIAGRAM B.43648

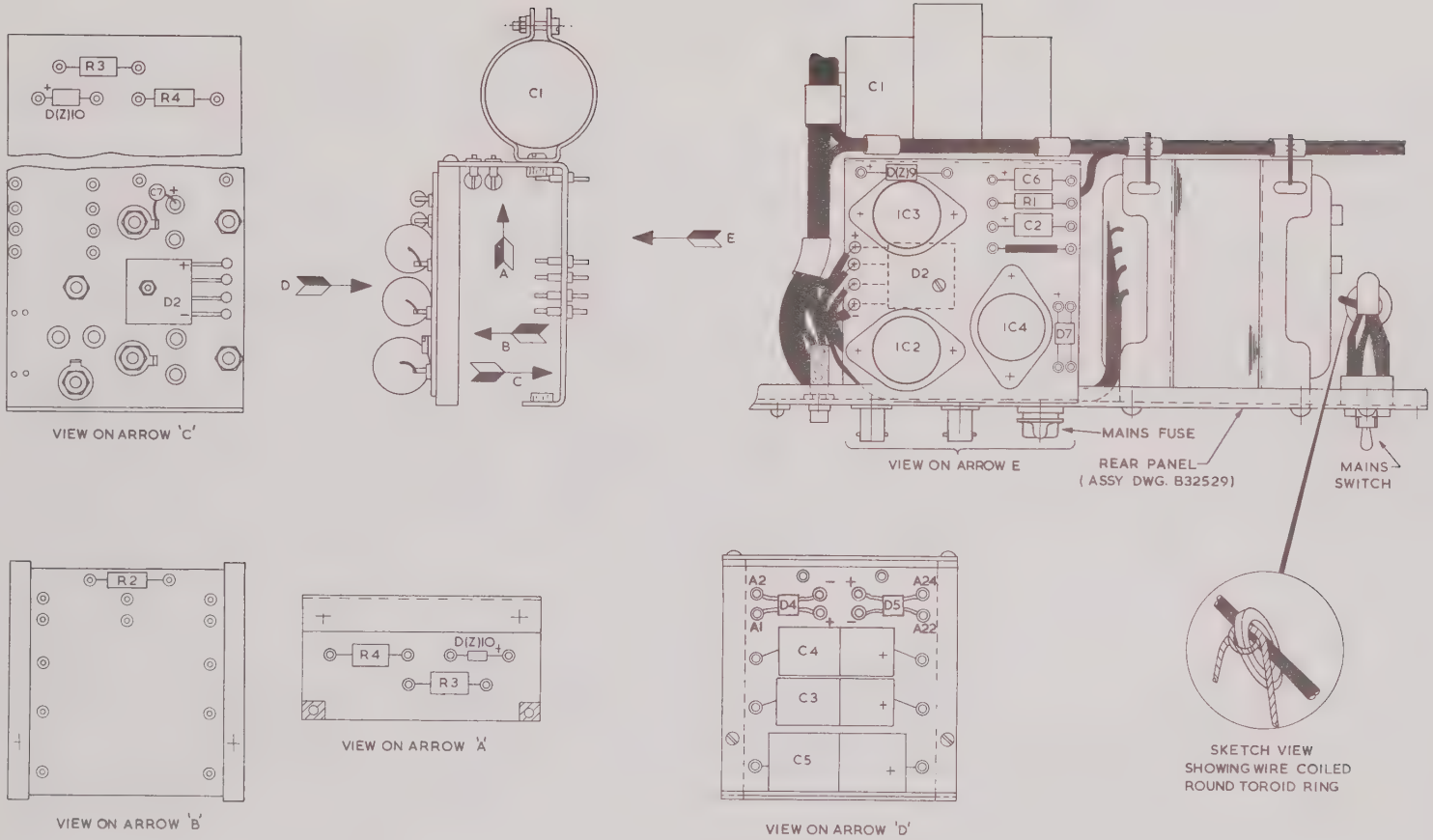


FIG.7 POWER SUPPLY-COMPONENT LAYOUT B43646

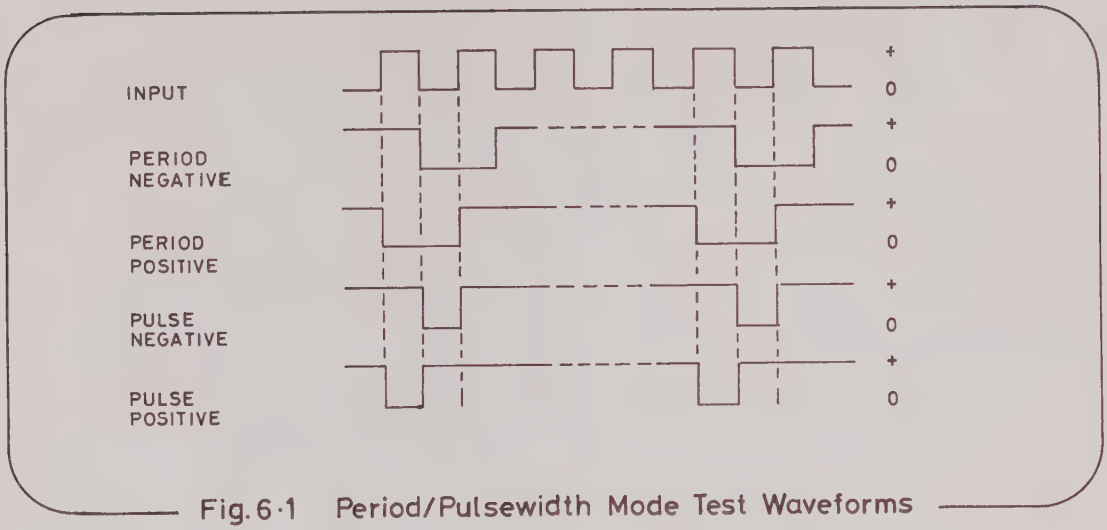


Fig.6·1 Period/Pulsewidth Mode Test Waveforms

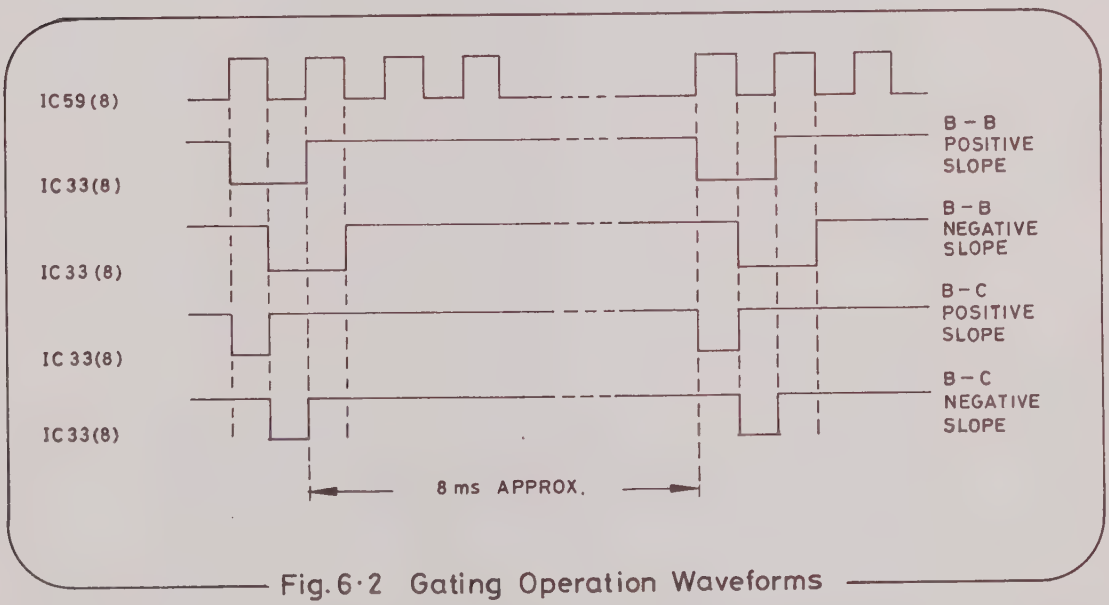


Fig.6·2 Gating Operation Waveforms

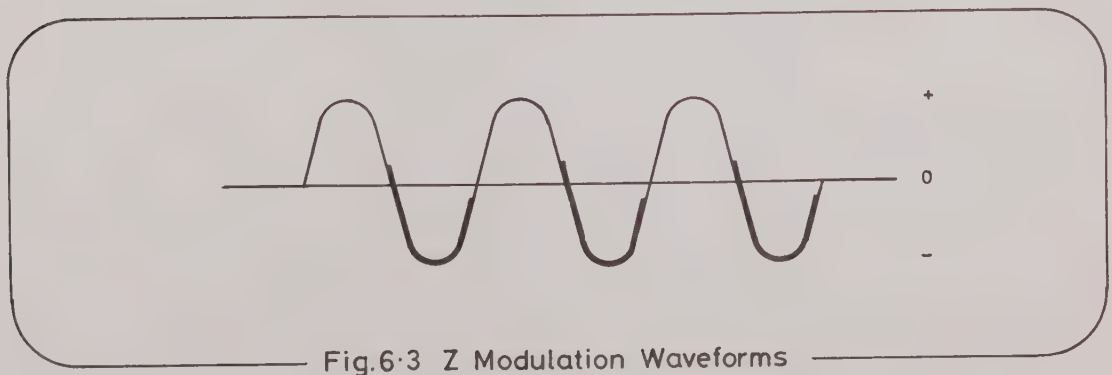


Fig.6·3 Z Modulation Waveforms

AMENDMENT LIST NO. 2

TO

TIMER COUNTER SERIES SM 202

MANUAL

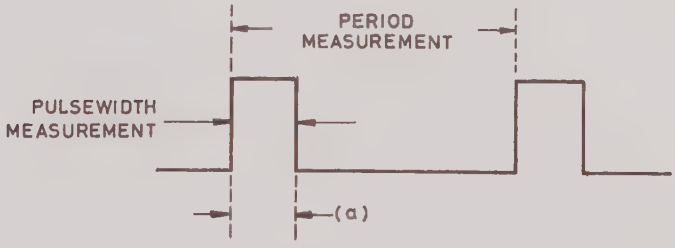
1. PURPOSE

The amendment contains information to convert the manual entitled 'Timer Counter Series SM 202,Issue 2,February 1973',to be suitable for Timer Counter Series SM 202M.

2. HAND AMENDMENTS

Section	Page	Para	Line	Change
Cover	-	-	-	'SM202' should read 'SM202M'
Title Page	-	-	-	'SM202' should read 'SM202M'
List of Contents	-	-	3	'SM202' should read 'SM202M'
	-	-	4	'SM202PB' should read 'SM202MPB'
1	1.2	Int.Clock Oscillator		Delete all information under the heading 'Accuracy'. Insert new specification as follows: (a) Type: Ovenaire OSC 73-11A (b) Long Term Stability: (i) At shipping(max): 5×10^{-8}/week (ii) After 45 days(max): 2×10^{-8}/week (iii)After 120 days(typical): 3×10^{-7}/year (c) Ambient Stability (-10°C to +55°C): 1×10^{-9}/°C (average) (d) Supply Voltage Stability (+15 V d.c. ± 15%): 5×10^{-9}/5% (e) Short Term Stability: 3×10^{-10} r.m.s./second over a 2 minute interval. (f) Warm-up Time: From a cold start at +25°C to within 5×10^{-7} of final stabilised frequency in 8 minutes approximately.
1	1.6	Active Probe Socket	2	Delete: SMA21 Insert: SMA21/M

Section	Page	Para	Line	Change
2	2.1	1.1	1	'SM202' should read,'SM202M'
2	2.2	Fig.2.1	-	Note that the COUNT,FREQ,PERIOD and AVERAGE PERIOD push-buttons on the SM202M instrument are engraved '(A I/P)'.
2	2.3	4.1	1	'SM202PB' should read, 'SM202MPB'
3	3.5	6.4	4	'-12 V d.c.' should read,'-5.2 V'
3	3.6	Fig.3.3	-	Note that the COUNT,FREQ,PERIOD and AVERAGE PERIOD push-buttons on the SM202M instrument are engraved '(A I/P)'.
3	3.11	7.2(d)	1	Change line 1 to read: 'This socket provides +12 V d.c. and -5.2 V d.c. supplies for use with.....'
3	3.11	7.2(d)	1 & 2	Delete: '..±12V ..' Insert:'..+12V & -5.2V ..' Delete: '..SMA21..' Insert:'..SMA21/M ..'
3	3.15	Fig.5.8		Re-draw this figure as shown below:



Minimum pulsewidth (a) for period measurements is 10ns and for pulsewidth measurements is 50ns

3	3.16 3.17 3.17	8.5.1(a) 8.6.1(a) 8.6.2(a)	Add to end of these paras: 'Turn DELAY TIME control fully anti-clockwise'.
3	3.18	8.7.1	Add to end of para: 'NOTE: Ensure that DELAY TIME control is fully anti-clockwise'.

Section	Page	Para	Line	Change
4	4.9	Fig.4.2		The waveform shown as the output of $\overline{Q}$ Monostable IC42 should be shown as a negative square wave.
4	4.13	5.2(c)		Delete: '-12 V Zener stabilised supply for the active probe supply socket. Insert: '+15 V unstabilised supply for the crystal oven'.
4	4.13	5.2(e)		Modify line (e) to read: '-5.2 V stabilised supply for the input amplifier board,display and logic board and the active probe socket'.
4	4.13	5.2(f)		Delete this line completely.
4	4.14	5.4	1	Delete: '..150 mA...' Insert: '..100 mA...'
			2	Delete: '...D5,D6,D8...'
4	4.14	5.5		Delete this paragrpah completely.
4	4.14	5.6		Re-number this paragraph as 5.5
4	4.14	5.7		Re-number this paragraph as 5.6
4	4.14	5.8		Delete this paragraph and insert new para, re-numbered 5.7 as follows: '+15 V Oven Supply. This is generated by winding W5. At switch-on,this supply provides a current of 500 mA (approx) to heat the crystal oven. Winding W3 is capable of supplying 500 mA for about 8 minutes'.
5	5.1	2.3.1	1	'SM202' should read 'SM202M'
5	5.2	4.2(c)	1	Delete: 'SM202...' Insert: 'SM202M...'
5	5.2	4.2(d)	Table	Delete all reference to -12.0 V supply rail, and limits of -11.4 V and -12.6 V. Insert reference to +15 V supply rail as follows:

Supply Rail	Min.	Max.
+15 V	+13.5 V	+16.5 V

5	5.2	4.2(e)	1	Delete: '..SM202..' Insert: '..SM202M...'
		4.2(f)	1	Delete: '..SM202..' Insert: '..SM202M...'

Section	Page	Para	Line	Change
5	5.3	4.2(g)	Table	Delete reference to -12.0 V Supply Rail. Insert reference to +15.0 V Supply Rail as follows:

Supply Rail	Test Point	Ripple limit(p-p)
+15 V	Pin 1 on oscillator X1	≯ 2 V p-p after 5 min warm-up time.

5	5.3	4.2(h)	DIAGRAM	Delete: '-12 V' Insert: '-5.2 V'
5	5.4	4.4(a)	Table	Delete capital letter 'M' from UNITS column of 'Period or Time' mode. Insert small 'm' in place of deleted'M' above.
5	5.6	4.7(n)	1	Delete: 'Operate...' Insert: 'With HOLD selected,operate...'
5	5.6	4.7(t)	1	Add to end of sentence: 'occurs'.
5	5.6	4.7(u)	5	Add to end of line the following sentence: 'Carry out step 4.14(h) and associated NOTE'.
5	5.6	4.7(v)	1	Delete: '...+12 V signal...' Insert: '...+1 V signal...'
5	5.6	4.7(w)	1	Delete: '..-2 V signal...' Insert: '..-1 V signal...'
5	5.6	4.7(y)	1	Delete: '...+2 V signal...' Insert: '...+1 V signal...'
5	5.6	4.7(z)	1	Delete: '...+2 V signal...' Insert: '...-1 V signal...'
5.	5.7	4.8(c)	2	Delete: '...+2 V signal...' Insert: '...+0.4 V signal...'
5	5.7	4.8(c)	4	Delete: '...+2 V signal...' Insert: '...+0.4 V signal...'
5	5.7	4.9(d)	2	Add to end of line: 'This should be > 100 MHz'.
5	5.7	4.9(e)	2	Add to end of line: 'This should be > 150 MHz'.
5	5.7	4.9(g)	2	Add to end of line: 'This should be > 100 MHz'.
5	5.8	4.13(c)	1	Delete: '...sginal...' Insert: '...signal...'
5	5.9	4.14(c)	2	Delete: '10 MHz' Insert: '12 MHz'
5	5.9	4.14(c)	2	Delete: '...osciloscope..' Insert: '...oscilloscope..'

Section	Page	Para	Line	Change
5	5.9	4.14(e)	1-2	Delete step (e) completely.
5	5.9	4.14(f)	1-2	Delete step (f) completely.
5	5.9	4.14(g)	1-2	Insert a full stop after 'sinewave'. Delete from 'noting' to end of sentence. Add new sentence as follows: 'Check that the display is stable up to 12 MHz'.
5	5.9	4.14(k)	1	Insert after '1 MHz': 'at 50 mV p-p'
5	5.10	4.15	Title	Delete title: 'Gating Mode' Insert new title: 'High Frequency Gating Operation'
5	5.10	4.15(a)	3	Delete: '10 MHz' Insert: 1 MHz'
5	5.10	4.15(a)	6	Add sentence to end of line: 'Increase frequency to 10 MHz and check that the waveforms are as shown in fig 6.2'
5	5.10	4.15(b)	1	Delete: 'With..' Insert: 'With DELAY TIME control fully anti-clockwise...'
5	5.10	4.15(b)	3	Delete: 'increases' Insert between 'for' and '30°': 'the first..' Insert after 'gradually': 'increases'
5	5.10	4.15(c)	2	Delete: 'waveforms' Insert: 'waveforms,as in (a) and (b) above'.
5	5.10	4.17(a)	2	Delete: 'reflection' Insert: 'distortion'
6	6.8	(Table 6.1)	27-28	Circuit Reference X1. Delete: SEL Part No:'WS28724,High Stability Oscillator,10 MHz,Cathodeon,FS5951' Insert new SEL Part No:WS60036,Precision Crystal Oscillator,10 MHz,Ovenaire OSC73-11A (Walmore Electronics Ltd)'
6	6.8	(Table 6.1)	29-30	Circuit Reference SK1. Delete: 'AS1529' Insert: 'AS1625' Delete: 'EZD27FS' Insert: 'EUD 14/14 GS'
6	6.11	(Table 6.2)	27	Circuit Reference R25. Delete: 'DS7259,Electrosil TR4,100k' Insert: 'DS33954,Mullard CR25,22k'
6	6.12	(Table 6.2)	2	Circuit Reference R41. Delete: DS 33945 Delete: 1 k. Insert: 220

Section	Page	Para	Line	Change
6	6.12 (Table 6.2)		21	Circuit Reference TR1. Delete: 'BS3044,Siliconix U257' Insert: ' - ,Siliconix 2N5912'

7 FIG 1. Display and Logic Board - Circuit Diagram E33155
Sheet A. Display Circuits and B/C Input Amplifiers.

Changes

Delete from above title: 'E 33155'
Add new Dwg.No: 'E 43651 sheet 1 of 2'.

Add circuit reference 'ILP3' to the OVER RANGE neon indicator.

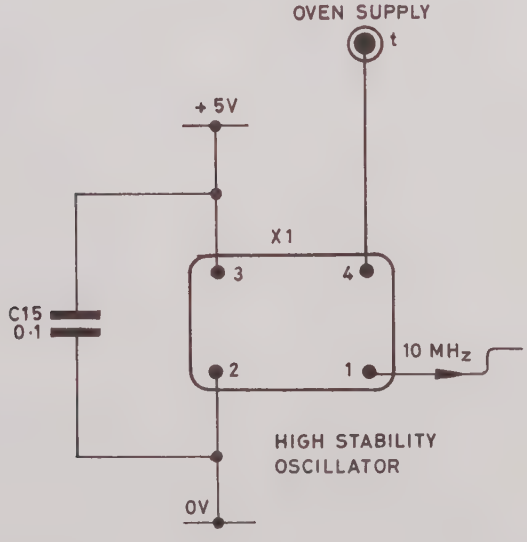
Add circuit reference 'SK1' adjacent to pins 5a,5b,4a,4b,3a,3b,2a,2b,1a,1b (labelled 'O/Ps'from 'A' Amplifier P.C.B.)

7 FIG. 1. Display and Logic Board - Circuit Diagram E 33155
Sheet B to G.

Changes

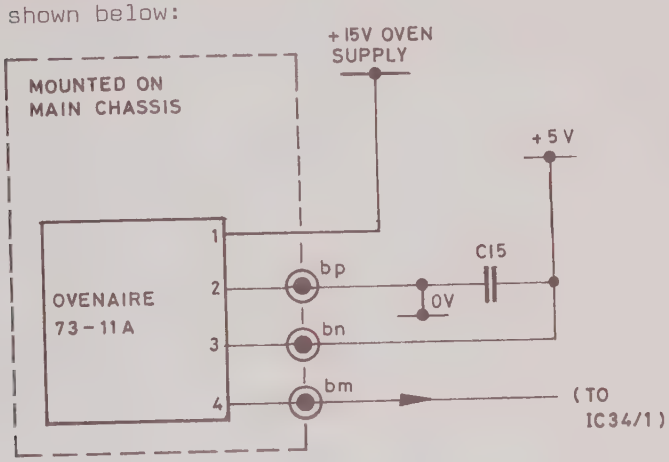
Delete from main title above (which appears on all sheets): 'E 33155'
Insert new Dwg.No: 'E 43651 sheet 2 of 2'.

Delete from diagram:



Changes

Insert new 'Ovenaire 73-11A' oscillator as shown below:



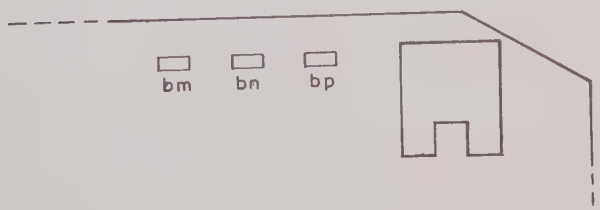
7 FIG 9. Display and Logic Board
BCD Fanout Board and Switchboard - Component Layouts

Changes

Delete sub-title: 'Switch Board B 33020/1'
Insert new sub-title: 'Switch Board B 43710'
Delete sub-title: 'Display and Logic Board E 33146/1'
Insert new sub-title: 'Display and Logic Board E 43644'

Delete the RENEWAL INSTRUCTIONS given for V1-V10.
Delete component C25 from Display and Logic Board layout diagram,and also associated note 'This component is fitted only on request'.

Delete the oscillator X1 component from the top right corner of the display and logic board layout diagram and re-draw as shown below:



		Changes
7	FIG 3. A Input Amplifier Boards - Circuit Diagram B 33156	Delete from main title: 'B 33156'. Insert new Dwg.No: 'B 43714' Transistor TR1 changed to type 2N 5912. Resistor R25 reduced to 22k. Board pin bm (connected to TR9 base) changed to bu. The 0 V line from junction of R34/R37 is now terminated at board pin bz,which in turn,is connected to chassis. Add this board pin (bz) to the 0 V line on the diagram. Resistor R41 reduced to 220Ω.
7	FIG 4. Input Amplifier Boards - Component Layout	Delete sub-title: 'Front End D 33148/1' Insert new sub-title: 'Front End D 43717'

3. **NEW PAGES**

SECTION 5. Insert new page 5.12

SECTION 6. Remove: Table 6.4 POWER SUPPLY (pages 6.15 and 6.16)
Insert: new Table 6.4 Power Supply

SECTION 7. Remove: fig 6 Power Supply - Circuit Diagram B 32528/2
fig 7 Power Supply - Component Layout B 32527

Insert: fig 6 Power Supply - Circuit Diagram B 43648
fig 7 Power Supply - Component Layout B 43646

SECTION 6

PARTS LIST

1. INTRODUCTION

1.1. This section contains information for ordering replaceable parts. Tables 6.1 to 6.4 provide the following information:

(a) Circuit reference

(b) Description

(c) Manufacturer/reference

(d) S.E. Laboratories part number

(e) Value, tolerance and rating for each component

1.2. Minor items, such as screws, nuts, etc., have not been included as they are not considered special to the equipment.

2. ORDERING INFORMATION

2.1. When ordering your replacement part, address the order to your local agent, or to **S.E. LABORATORIES, (Engineering) Ltd., Service Department, North Feltham Trading Estate, Feltham, Middlesex, England. Telephone: Feltham 1166/5876, or Northern Sales Office, Telephone Number, Sandiacre 3255.**

2.2. Specify the following information, for each part:

(a) Model and serial number of the equipment

(b) Part number

(c) Circuit reference

(d) Description

2.3. To order a part not listed give the part number, description of the next higher assembly which is not listed and a complete description of the part required.

2.4. The assemblies are listed as follows:-

Table	
6-1	Display and Logic Board.
6-2	Input Amplifier
6-3	BCD Fan Out and Programmer Unit SM248
6-4	Power Supply

TABLE 6.1 DISPLAY & LOGIC BOARD (Refer to the circuit diagram)

Cct. Ref.	S.E.L. Part No.	Manufacturer/Reference	Value	Tol ± %	Rating
		Capacitors (μF)			
C1	CS 31012	Erie, NPO/YD	10p	10	200V
C2	As C1				
C3	CS 31167	Erie, 811/4700	4700p	20	
C4	As C3				
C5	CS 31162	Erie, 390	68p	10	100V
C6	As C5				
C7	CS 31011	Erie, YD/K120051/470p	470p	10	
C8	As C7				
C9	CS 30343	Erie, 811/T/30V	0.1	+50, -25	30V
C10	As C9				
C11	CS 30899	Erie, YD/P100	4.7p	±¼p	200V
C12	As C11				
C13	As C9				
C14	As C9				
C15	CS 30620	Mullard, C280AE/P100K	0.1	20	250V
C16	CS 30602	Wima, MKS	0.47	20	100V
C17	As C16				
C18	CS 31165	Mullard, C421, AM/DP22	22	20	15V
C19	CS31164	Erie, 390	470p	10	100V
C21	As C19				
C22	CS 31163	Erie, 390	100p	10	100V
C23	CS 30225	Mullard, C426AR/B64	64	+50, -10	4V
C24	As C15				
C25					
C26	As C9				
C27					
C28 thru C57	CS 30566	Erie, 831/T/25V	0.01	+50, -25	25V
C58	CS 31325	I.T.T., Tag 22/6.3	22	20	6.3V
C59	As C58				
C60	CS 31012	Erie, NPO/YD	10p	10	
		Diodes			
D1	BS 2522	Mullard, BYX 10			
D2	As D1				
D3	As D1				
D4 thru D13	BS 2045	Mullard, 1N914			
D14	BS 2879	Mullard, 1N4009			
D15	As D14				

Table 1 (Cont'd.)

Cct. Ref.	S.E.L. Part No.	Manufacturer/Reference	Value	Tol ± %	Rating
		Integrated Circuits			
IC1	BS 7476	Texas, SN7486N			
IC2	BS 7400	Texas, SN 7400 N			
IC3	BS 7402	Texas, SN 7402N			
IC4	BS 7541	Texas, SN 74141N			
IC5	As IC2				
IC6	BS 7410	Texas, SN 7410N			
IC7	As IC4				
IC8	As IC4				
IC9	BS 7475	Texas, SN 7475N			
IC10	As IC4				
IC11	As IC9				
IC12	BS 7490	Texas, SN 7490			
IC13	As IC4				
IC14	As IC9				
IC15	As IC12				
IC16	As IC4				
IC17	As IC9				
IC18	As IC12				
IC19	As IC4				
IC20	As IC9				
IC21	As IC12				
IC22	As IC4				
IC23	As IC9				
IC24	As IC12				
IC25	As IC4				
IC26	As IC9				
IC27	As IC12				
IC28	As IC4				
IC29	As IC9				
IC30	As IC12				
IC31	As IC2				
IC32	BS 7473	Texas, SN 7473N			
IC33	BS7413	Texas, SN 7413N			
IC34	BS7404	Texas, SN 7404N			
IC35	As IC12				
IC36					
IC37	As IC2				
IC38	As IC2				
IC39	BS 7451	Texas, SN 7451N			
IC40	As IC2				

Table 6.1 (cont'd).

Cct. Ref.	S.E.L. Part No.	Manufacturer/Reference	Value	Tol ± %	Rating
IC41	As IC2				
IC42	BS7522	Texas, SN 74122N			
IC43	As IC2				
IC44	As IC12				
IC45	As IC32				
IC46	As IC12				
IC47	As IC6				
IC48	As IC32				
IC49	As IC2				
IC50	As IC12				
IC51	As IC6				
IC52	BS7440	Texas, SN 7440N			
IC53	As IC12				
IC54	As IC2				
IC55	As IC2				
IC56	As IC12				
IC57	As IC6				
IC58	As IC2				
IC59	BS 7420	Texas, SN 7420N			
IC 60	BS 3008	Texas, SN 74S112N			
IC61	As IC12				
IC62	As IC32				
IC63	As IC2				
IC64	As IC32				
IC65	BS 7551	Texas, SN 74151N			
IC66	As IC12				
IC67	As IC12				
IC68	BS 3050	Texas, SN 74S64N			
IC69	As IC34				
IC70	As IC34				
IC71	As IC2				
IC72	As IC2				
		Resistors, Fixed (Ω)			
R1	DS 33956	Mullard, CR25	82 k	5	¼W
R2	DS 33957	Mullard, CR25	120 k	5	¼W
R3	DS 33950	Mullard, CR25	6.8 k	10	¼W
R4	DS 34037	Mullard, CR25	27 k	5	¼W
R5	As R3				
R6	As R4				
R7	DS 33951	Mullard, CR25	10 k	5	¼W
R8	As R3				
R9	As R4				
R10	As R4				

Table 6.1. (cont'd.)

Cct. Ref.	S.E.L. Part No.	Manufacturer/Reference	Value	Tol ± %	Rating
R11	As R4				
R12	As R4				
R13	As R4				
R14	As R4				
R15	As R4				
R16	As R4				
R17	DS 33958	Mullard, CR25	150k	5	¼W
R18	As R3				
R19	DS 32573	Electrosil, TR5	1M	5	¼W
R20	As R19				
R21	DS 33530	Mullard, MR25	511	1	¼W
R22	As R21				
R23	DS 33998	Mullard, CR25	15	5	¼W
R24	As R23				
R25			22k		¼W
R26			22k		¼W
R27	DS 34029	Mullard, CR25	5.6k	5	¼W
R28	As R27				
R29	DS 34010	Mullard, CR25	150	5	¼W
R30	As R29				
R31	DS 33945	Mullard, CR25	1k	10	¼W
R32	As R31				
R33	DS 34221	Electrosil, TR5	910k	2	¼W
R34	DS 34219	Mullard, MR25	18.2k	1	¼W
R35q	DS 34218	Mullard, MR25	7.5k	1	¼W
R36	As R33				
R37	As R34				
R38	As R35				
R39	DS 34220	Mullard, MR25	90.9k	1	¼W
R40	DS 34060	Mullard, MR25	12.1k	1	¼W
R41	As R39				
R42	As R40				
R43	DS 33944	Mullard, CR 25	560	10	¼W
R44	DS 33877	Mullard, MR25	3.01k	1	¼W
R45	As R44				
R46	DS 34216	Mullard, MR25	301	1	¼W
R47	As R43				
R48	As R44				
R49	As R44				
R50	As R46				

Table 6.1. (con'td.)

Cct. Ref.	S.E.L. Part No.	Manufacturer/Reference	Value	Tol ± %	Rating
R51	DS34217	Mullard, MR25	3.57 k	1	¼W
R52	DS 33533	Mullard, MR25	750	1	¼W
R53	As R51				
R54	As R52				
R55	As R34				
R56	DS 33536	Mullard, MR25	1.21k	1	¼W
R57	As R34				
R58	As R56				
R59	DS34019	Mullard, CR25	820	10	¼W
R60	DS33939	Mullard, CR25	33	10	¼W
R61	As R60				
R62	DS 33942	Mullard, CR25	330	10	¼W
R63	As R62				
R64	As R59				
R65	As R60				
R66	As R60				
R67	As R62				
R68	As R62				
R69	DS 33947	Mullard, CR25	2.2 k	10	¼W
R70	As R69				
R71	DS 33954	Mullard, CR25	22k	10	¼W
R72	As R71				
R73	As R31				
R74	DS 33837	Mullard, CR 25	100	10	¼W
R75	As R31				
R76	As R31				
R77	DS 33956	Mullard, CR25	82k	10	¼W
R78	DS 34037	Mullard, CR25	27k	10	¼W
R79	DS 33943	Mullard, CR25	470	10	¼W
R80	DS 33949	Mullard, CR25	4.7k	10	¼W
R81	As R77				
R82	DS 34007	Mullard, CR25	82	10	¼W
R83	DS 34013	Mullard, CR25	270	10	¼W
R84	As R69				
R85	As R69				
R86	As R60				
R87					
R88	As R31				
R89	As R83				
R90	As R3				

Table 6.1 (Cont'd)

Cct. Ref.	S.E.L. Part No.	Manufacturer/Reference	Value	Tol ± %	Rating
R91	As R17				
R92	As R31				
R93	As R31				
R94	As R17				
R95	As R3				
R96	DS 33949	Mullard, CR25	4.7k	10	¼W
R97	As R96				
R98	As R96				
R99	As R96				
R100	As R96				
R101	As R96				
R102	As R96				
R103	As R96				
R104	As R96				
R105	As R96				
R106	As R96				
R107	As R96				
R108	As R96				
R109	As R96				
R110	DS 34018	Mullard, CR 25	680	10	¼W
R111	As R78				
R112	As R31				
R113	DS 33537	Mullard, MR25	1.5k	1	¼W
R114	DS 33530	Mullard, MR25	511	1	¼W
R115	As R114				
R116	As R113				
R117	As R114				
R118	As R114				
R119	DS 33945	Mullard, CR25	1k	10	¼W
R120	DS 33529	Mullard, MR25	475	1	¼W
R121	As R120				
		Resistors, Variable (Ω)			
RV1	FS 10503		500	10	
RV2	As RV1				
RV3	FS 10504		10k	10	

Table 6.1. (cont'd).

Cct. Ref.	S.E.L. Part No.	Manufacturer/Reference	Value	Tol ± %	Rating
		Transistors			
TR1	BS 2886	Mullard, BSX21			
TR2	As TR1				
TR3	BS 3043	R.C.A., 40346			
TR4	As TR1				
TR5	BS 2901	Siliconix, U 235			
TR6	As TR5				
TR7	BS 2882	R.C.A., CA 3046			
TR8	As TR7				
TR9	As 2838	Motorola, MPS 3640			
TR10	As TR9				
TR11	As TR9				
TR12	As TR9				
TR13	BS 2599	Mullard, BSX20			
TR14	As TR7				
TR15	As TR 13				
TR16	As TR13				
TR17	BS 2519	Mullard, BCY 72			
TR18	As TR17				
TR19	As TR13				
TR20	As TR1				
TR21	As TR1				
		Miscellaneous			
V1	WS 28804	Character Indicator Tube I.T.T., 58GA-S			
V2	WS 28805	Character Indicator Tube, I.T.T., 58GR-S			
V3 thru V10	WS 28782	Numerical Indicator Tube, I.T.T., 5870-L			
X1	WS 28724	High stability oscillator, 10MHz, Cathodeon, FS 5951			
SK1	AS 1529	28-way edge connector, Ferranti, EZD 27FS			
SK2	AS 1530	50-way edge connector, Ferranti, EZD53FW.			
EXT CLOCK Z MOD INPUT B,C	AS 1442	BNC Socket, P.E.T., 742/PTFE/ MOD/SEL.			

Table 6.1. (Cont'd.)

Cct. Ref.	S.E.L. Part No.	Manufacturer/Reference	Value	Tol ± %	Rating
INPUT B INPUT C SENS.SW.	QS 22344	Switch; Elma/Radiatron 01-2x3 HOA DIG.			
P/PW+–	QS 22345	Switch, Elma/Radiatron 01-2x4 HOA DIG.			
±MAN	QS22291	Switch, toggle, D.P.D.T. Waycom, MST 205TA			
EXT. PROG. GATE OPEN OVER RANGE	JS 14070	Neon indicator, West Hyde Development			
RANGE SW.	D32463	L.H. Switchbank S.E.L.			
	D32465	Centre switchbank, S.E.L.			
	D32464	R.H. Switchbank, S.E.L.			

TABLE 6.2. 'A' INPUT AMPLIFIER (Refer to the circuit diagram)

Cct. Ref.	S.E.L. Part No.	Manufacturer/Reference	Value	Tol ± %	Rating
		Capacitors (μF)			
C1	CS 4136	Waycom, Tropyfol F	0.022	20	400V
C2	CS 31170	Erie, P100/YD	3.3p	±0.5p	200V
	CS 30907	Erie, YD/NPO	22p	10	–
C3	CS 31171	Erie, P100/YD.	2.4p	±0.5p	200V
C4	CS 31174	Erie, 361/K120051	500p	25	
C5	CS 31010	Erie, K170051/YD	1000p	10	200V
C6	CS 30343	Erie, 811/T/30V	0.1	+50, -25	30V
C7	CS 31092	Erie, SN 1300/YD	150p	10	200V
C8	CS 31166	Erie, 811/T/30V	0.047	+50, -25	30V
C9	As C6				
C10	As C5				
C11	As C8				
C12	As C6				
C13	CS 30899	Erie, P100YD	4.7p	±0.5p	200V
C14	As C5				
C15	CS 31012	Erie, NPO/YD	10p	10	200V
C16	CS 30900	Erie, K120051/YD	1000p	10	200V
C17	CS 31166	Erie, 831/T/30V	0.047	+50 -25	30V
C18	CS 30566	Erie, 831/T/25V	0.01	+50 -25	25V
C19	As C18				
C20	CS 30343	Erie, 811/T/25V	0.1	+50 -20	25V
		Diodes			
D1	BS 2045	Mullard, 1N914			
D2	As D1				
D3	BS 2879	Mullard, 1N4009			
D4	As D3				
D5	As D3				
		Integrated Circuits			
IC1	BS 2885	Motorola, MC 1010P			
IC2	BS 3053	Motorola, MC 1039P			
IC3	BS 3052	Motorola, MC 1034			
IC4	BS 3051	Motorola, MC 1032			
IC5	BS 2883	Motorola, MC 1014			
IC6	BS 3054	Motorola, MC10102P			
IC7	As IC4				
IC8	BS 2884	Motorola, MC 1013P			
IC9	As IC2				

Table 6.2 (cont'd.)

Cct. Ref.	S.E.L. Part No.	Manufacturer/Reference	Value	Tol ± %	Rating
IC10	As IC1				
		Resistors fixed (Ω)			
R1	DS34000	Mullard, CR25	22	5	¼W
R2	DS 34221	Electrosil, TR5	910k	2	¼W
R3	DS 33835	Electrosil, TR5	110k	2	¼W
R4	DS 34003	Mullard, CR25	39	10	¼W
R5	As R1				
R6	DS 33962	Mullard, CR25	1M	5	¼W
R7	DS 6714	Electrosil, TR4	10K	5	¼W
R8	DS 32366	Electrosil, TR5	100k	2	¼W
R9	As R6				
R10	DS 34004	Mullard, CR25	47	10	¼W
R11	DS 33536	Mullard, MR25	1.21k	1	¼W
R12	DS 33532	Mullard, MR25	681	1	¼W
R13	DS 33531	Mullard, MR25	619	1	¼W
R14	DS 33942	Mullard, CR25	330	10	¼W
R 15	DS 6506	Electrosil, TR4	2.2k	5	¼W
R16	DS 33533	Mullard, MR25	750	1	¼W
R17	DS 33998	Mullard, CR25	15	10	¼W
R18	As R17				
R19	DS 33525	Mullard, MR25	200	1	¼W
R20	As R17				
R21	As R16				
R22	As R15				
R23	As R11				
R24	DS 34057	Mullard, CR25	4.7M	10	¼W
R25	DS 7259	Electrosil, TR4	100k	5	¼W
R26	As R6				
R27	DS 33876	Mullard, MR25	1k	1	¼W
R28	DS 33524	Mullard, MR25	162	1	¼W
R29	DS 33997	Mullard, CR25	12	10	¼W
R30	DS 33528	Mullard, MR25	332	1	¼W
R31	As R28				
R32	DS 34001	Mullard, CR25	27	10	¼W
R33	As R27				
R34	DS 33522	Mullard, MR25	82	1	¼W
R35	DS 33534	Mullard, MR25	825	1	¼W
R36	DS 33527	Mullard, MR25	267	1	¼W
R37	DS 33515	Electrosil, TR4	110	5	¼W
R38	DS 33537	Mullard, MR25	1.5k	1	¼W
R39	DS 33943	Mullard, CR25	470	5	¼W

Table 6.2 (cont'd.)

Cct. Ref.	S.E.L. Part No.	Manufacturer/Reference	Value	Tol ± %	Rating
R40	As R39				
R41	DS 33945	Mullard, CR25	1k	5	¼W
R42	As R38				
R43	DS 33530	Mullard, MR25	511	1	¼W
R44	As R43				
R45	As R38				
R46	As R43				
R47	As R43				
R48	As R38				
R49	As R43				
R50	As R43				
R51	As R41				
R52	R41				
R53	DS 33876	Mullard , MR25	1k	1	¼W
R54	DS 33539	Mullard, MR25	5.11k	1	¼W
R55	DS 33524	Mullard, MR25	162	1	¼W
R56	DS 33538	Mullard, MR25	2.21k	1	¼W
		Resistors, Variable (Ω)			
RV	FS 10502	Level, potentiometer	10k	10	
		Transistors			
TR1	BS 3044	Siliconix, U257			
TR2	BS2835	Motorola, 2N 5179			
TR3	As TR2				
TR4	As TR2				
TR5	As TR2				
TR6	As TR2				
TR7	BS 2838	Motorola, MPS 3640			
TR8	As TR7				
TR9	As TR2				
TR10	As TR2				
TR11	As TR2				
TR12	BS2599	Mullard, BSX20			
		Miscellaneous			
A INPUT Z MOD	AS 1442	Socket, BNC, P.E.T. 742/PTFE/MOD/SEL			

Table 6.2 (cont'd).

Cct. Ref.	S.E.L. Part No.	Manufacturer/Reference	Value	Tol ± %	Rating
A SENS SW	QS 22371	Switch, S.E.L., D 32479			
AC/DC	QS 22244	Switch, toggle, waycom, MST 105D			
	CS 31173	Capacitor 470μF, -10%, +5%, 6.3V Mullard, 01613471			
FX	GS 11197	Ferroxcube bead, Mullard FX 1115			
	GS 11208	Ferrite bead, Neosid, 3.5 x 1.2 x 3, F14 (for TR11).			

TABLE 6.3 BCD FANOUT AND PROGRAM UNIT SM 248 (Refer to the circuit diagram)

Cct. Ref.	S.E.L. Part No.	Manufacturer/Reference	Value	Tol ± %	Rating
		Capacitors (μF)			
C1	CS 30647	Erie, X5U/8101 - 025	1000p	+30, -20	30V
C2	CS 30166	Mullard, C280AE/P100K	0.1	20	250V
		Diodes			
DZ1	BS2525	Mullard, BZY88, C6V2			
		Integrated Circuits			
IC1	BS 7400	Texas, SN 7400N			
IC2	BS 7521	Texas, SN 74121N			
IC3	BS 7408	Texas, SN 7408N			
IC4	As IC3				
IC5	As IC3				
IC6	As IC3				
IC7	As IC3				
IC8	As IC3				
IC9	As IC3				
IC10	As IC3				
IC11	As IC3				
IC12	As IC1				
IC13	BS 7412	Texas, SN 7412N			
IC14	BS 2727	Texas, SN 7401N			
IC15	As IC14				
IC16	BS 7404	Texas, SN 7404N			
IC17	As IC14				
IC18	As IC16				
IC19	As IC14				
		Resistors (Ω)			
R1	DS 33950	Mullard, CR25	6.8k	10	¼W
		Miscellaneous			
FS1	RS 23125	Fuse, 250mA, Bulgin F290			
PROG.I/P	AS 0608	Plug, Fixed, 18-way, M^{c}Murdo MP 118.			
BCD O/P	AS 1521	Socket, fixed, 50-way M^{c}Murdo MS 150			

TABLE 6.4. POWER SUPPLY (Refer to the circuit diagram)

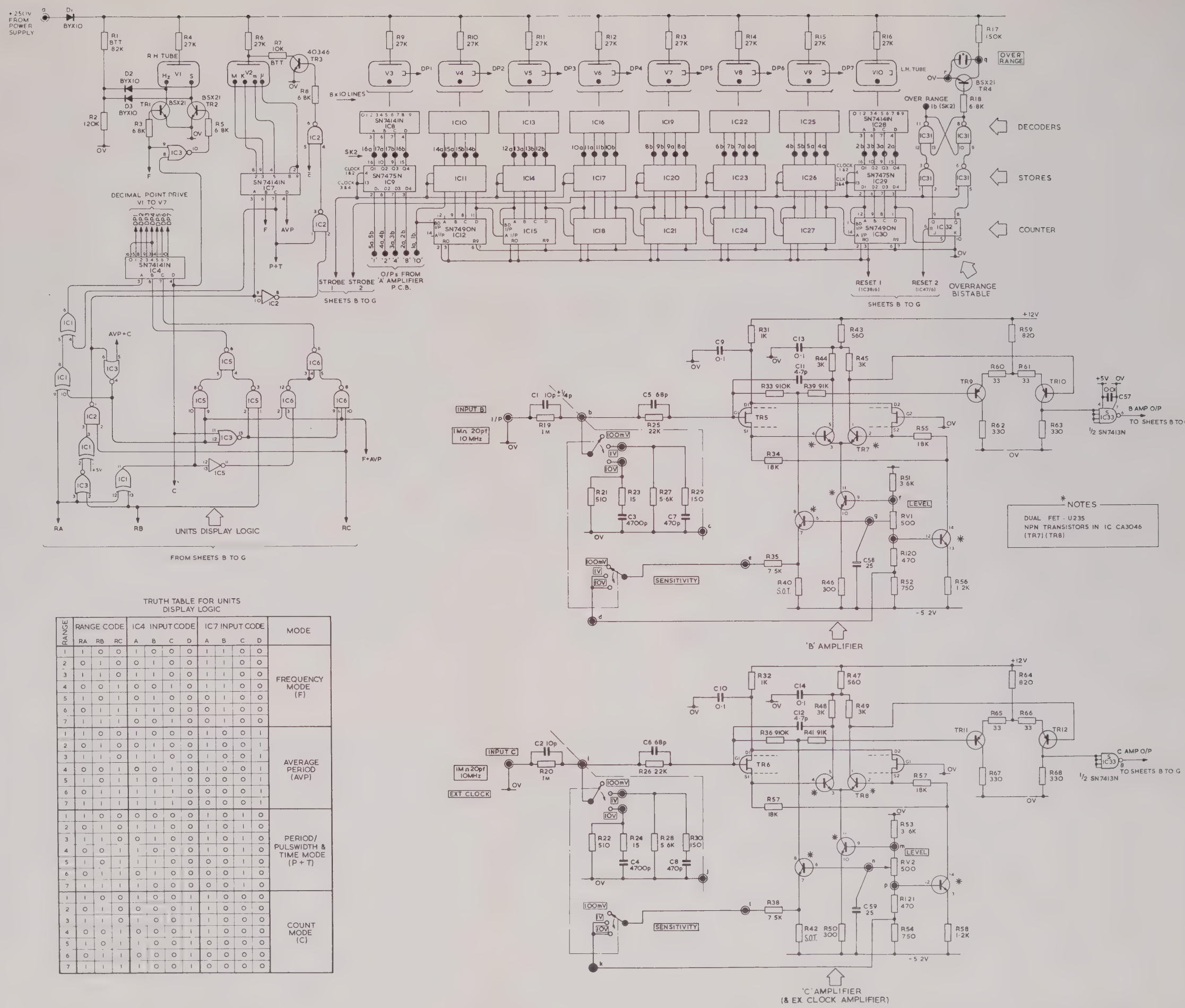
Cct. Ref.	S.E.L. Part No.	Manufacturer/Reference	Value	Tol ± %	Rating
		Capacitors (μF)			
C1	CS 31172	Mullard, 106 15103	10,000	+50, -10	16V
C2	CS 30176	Mullard, 426AR/E10	10	+50, -10	16V
C3	CS 31169	Erie, 21104/100/0471/0A/0400	470		
C4	As C3				
C5	CS 31168	Erie, 21106/100/0222/0A/0160	2,200		16V
C6	As C2				
C7	As C2				
		Diodes			
D1					
D2	BS 3057	Motorola, MDA 970A-1			
D3					
D4	BS 2427	Motorola, 1N4001			
D5	As D4				
D6	As D4				
D7	BS 2365	Motorola, MDA 920A -2			
D8	As D4				
D(z)2	BS 3059	Motorola, 1N5333A			
D(z)9	BS 3058	Motorola, 1N 5348A			
		Integrated Circuits			
IC2	BS 3055	S.G.S. Fairchild, L005			
IC3	BS 3056	S.G.S. Fairchild, LO36			
IC4	As IC2				
		Resistors (Ω)			
R1	DS 34000	Mullard, CR25	22	5	¼W
R2	DS 34222	Welwyn, W21	68	5	2.5W
		Welwyn, W21	56	5	2.5W
		Welwyn, W21	82	5	2.5W
		Miscellaneous			
FS1	RS 23113	Fuse Link, 250mA, Beswick,TDC123			
	RS 23064	Fuse Holder, Britempex FEP704M/70G			
	AS 0450	Plug, Greenpar BN1/5			
SKT 1	AS 1398	Socket, 3 pin, fixed, Electro Methods SM35-N			

Table 6.4 (cont'd).

Cct. Ref.	S.E.L. Part No.	Manufacturer/Reference	Value	Tol ± %	Rating
SW1	QS 22230	Switch, mains, Painton, 22/10/0201/00			
	ES 8456	Transformer mains, Ripley, S.E.L. 5/397			
	ES 8377	Transformer, 5/358, Buckingham Electronic			
	GS 11167	Toroid, FX007, Mullard, 240V			

SECTION 7

CIRCUIT DIAGRAMS & COMPONENT LAYOUTS



NOTES

DUAL FET - U235
NPN TRANSISTORS IN IC CA3046
(TR7) (TR8)

TRUTH TABLE FOR UNITS DISPLAY LOGIC

RANGE	RANGE CODE			IC4 INPUT CODE				IC7 INPUT CODE				MODE
	RA	RB	RC	A	B	C	D	A	B	C	D	
1	1	0	0	1	0	0	0	1	1	0	0	FREQUENCY MODE (F)
2	0	1	0	0	1	0	0	1	1	0	0	
3	1	1	0	1	1	0	0	1	1	0	0	
4	0	0	1	0	0	1	0	1	1	0	0	
5	1	0	1	0	1	0	0	0	1	0	0	
6	0	1	1	1	1	0	0	0	1	0	0	
7	1	1	1	0	0	1	0	0	1	0	0	
1	1	0	0	1	0	0	0	1	0	0	1	AVERAGE PERIOD (AVP)
2	0	1	0	0	1	0	0	1	0	0	1	
3	1	1	0	1	1	0	0	1	0	0	1	
4	0	0	1	0	0	1	0	1	0	0	1	
5	1	0	1	1	0	1	0	0	0	0	1	
6	0	1	1	1	1	1	0	0	0	0	1	
7	1	1	1	1	1	1	0	0	0	0	1	
1	1	0	0	0	0	0	0	1	0	1	0	PERIOD/ PULSWIDTH & TIME MODE (P + T)
2	0	1	0	1	1	0	0	1	0	1	0	
3	1	1	0	0	1	0	0	1	0	1	0	
4	0	0	1	1	0	0	0	1	0	1	0	
5	1	0	1	1	1	0	0	0	0	1	0	
6	0	1	1	0	1	0	0	0	0	1	0	
7	1	1	1	1	0	0	0	0	0	1	0	
1	1	0	0	1	0	0	1	1	0	0	0	COUNT MODE (C)
2	0	1	0	0	0	0	1	1	0	0	0	
3	1	1	0	1	0	0	1	1	0	0	0	
4	0	0	1	0	0	0	1	1	0	0	0	
5	1	0	1	1	0	0	1	0	0	0	0	
6	0	1	1	0	0	0	1	0	0	0	0	
7	1	1	1	1	0	0	1	0	0	0	0	

FIG. 1 DISPLAY & LOGIC BOARD - CIRCUIT DIAGRAM E33155
SHEET A. DISPLAY CIRCUITS AND B/C INPUT AMPLIFIERS

SHEET B. FREQUENCY MODE
(WITH VARIABLE DISPLAY CIRCUIT)

NOTES

1. INDICATES WIRING POINT
2. SK1 INDICATES CONNECTION TO INPUT AMP BOARD.
3. SK2 INDICATES CONNECTION TO BCD/ PROGRAM BD.
4. C-C INCL ARE 0·01 μF.
5. DE-COUPLING CAPACITORS BETWEEN 0V & +5V.
6. ALL BISTABLES ARE SN7473N UNLESS OTHERWISE STATED (SN74112N, IC)
7. ALL RESISTORS ARE MORGANITE XL 1/4W ± 10% UNLESS OTHERWISE STATED.

CHANNEL SELECT 1/P2 STOP

POLARITY SELECTION GATES

RANGE SELECTION CIRCUIT

TIME BASE (DIVIDER) LOGIC

SWITCH BANK

HIGH STABILITY OSCILLATOR

TRANSFER BISTABLE

RESET BISTABLE

GATE OPEN BISTABLE (F, AVP, MODES)

GATE OPEN BISTABLE (P/PW, T, C MODES)

STOP BISTABLE

AUTOMATIC RESET

CONTROL LOGIC

VARIABLE DELAY

SCHMITT TRIGGER

TIME & COUNT GATING LOGIC

INPUT C LOGIC

INPUT B LOGIC

B & C POLARITY SWITCH (REAR VIEW)

'EX OR' GATES SN 7486N

FIG. 1 DISPLAY AND LOGIC BOARD - CIRCUIT DIAGRAM E33155

SHEET C. PERIOD/PULSEWIDTH MODES
(WITH VARIABLE DISPLAY CIRCUIT)

NOTES

1. INDICATES WIRING POINT
2. SK1 INDICATES CONNECTION TO INPUT AMP BOARD.
3. SK2 INDICATES CONNECTION TO BCD/PROGRAM BD.
4. C-C INCL. ARE 0·01 µF.
5. DE-COUPLING CAPACITORS BETWEEN OV & +5V.
6. ALL BISTABLES ARE SN7473N UNLESS OTHERWISE STATED (SN74112N, IC)
7. ALL RESISTORS ARE MORGANITE XL 1/4W ± 10% UNLESS OTHERWISE STATED.

CHANNEL SELECT I/P2 STOP

SK1 7a 7b 6a 6b 9a 8a 8b 11a 11b

F+CR1 OV

R113 1·5K R114 510 D14 IN4009 C25 S.O.T. -5·2V

R113 510 RESET 3

R116 1·5K R117 510 D15 IN4009 -5·2V R118 510 (Y) IC47/12

AMP o/p AMP o/p

SK1 9b 10b

+5V R92 1K R93 1K -V +V

IC68 SN74564N P̄ OV

POLARITY SELECTION GATES

SK1 SK2

12a 27b aq OV

27a ah +5V

13b aj +12V } P.S. CONNECTIONS

12b ak -5·2V

14a al Z MOD o/p

RANGE SELECTION CIRCUIT

SN7415IN IC65 STROBE OV RA RB RC RANGE CODE I/P

SWITCH BANK

SK2 24a am EXCP EXCP H̄ BC̄ 23a an 24b ap

IC69 R96 4·7K R97 4·7K R98 4·7K

RESET EXT CLOCK HOLD B-C B-B

T̄ 23b aq AVP AVP P P̄ F F̄ C C̄ IC71 25b ar 21a as 26b at 19b au

R99 4·7K R100 4·7K R101 4·7K R102 4·7K R103 4·7K

TIME AVERAGE PER OD FREQUENCY COUNT

RC RB RA S TOT IC70 20b av 21b aw 22b ax 22a ay 20a az 19a ba

R104 4·7K R105 4·7K R106 4·7K R107 4·7K R108 4·7K R109 4·7K

STORED TOTAL EXT PROG

C26 0·1 PROG 25a bc bd R119 1K

TIME BASE (DIVIDER) LOGIC

SN7490N IC44 IC46 IC50 IC53 IC56 IC61 IC66 IC67

+5V R69 2·2K TR13 BSX20 R70 2·2K 1MHz REF o/p OV OVEN SUPPLY 1MHz (IC34/8)

C15 0·1 X1 10 MHz HIGH STABILITY OSCILLATOR IC34

SN 7490N IC35 1MHz 2MHz 2MHz 1MHz

F P+T EXCP EXCP IC38 IC39 IC41 IC34

IC49 AVP+C AVP IC59/6 IC49 AVP

IC54 IC51 IC60 F+AVP SN74S112N (+V PULSE)+(-V PULSE)+T+C CONTROL LOGIC

GATE OPEN BISTABLE (F, AVP, MODES) GATE OPEN BISTABLE (P/PW, T, C MODES)

RESET 3 (TO R115) IC49§ TRANSFER BISTABLE IC59 IC48 IC39 T+C H

GATE OPEN IC63 IC51 IC55 IC45/1 IC45/5 2MHz 1MHz STOP BISTABLE RESET BISTABLE

+250V R91 150K BTT R90 6·8K TR20 BSX20 C24 0·1 OV

+5V AUTOMATIC RESET D8 C23 64µ 4V OV IC57 SK2 R EXT. PROG. TR21 BSX21 R94 150K BTT R95 6·8K

IC62 ac R ad R̄ C22 100 OV

R71 22K C16 0·47µ D12 IC42 SN74122N (ONE SHOT)

+12V R110 680 DELAY OR RV3 10K R81 82K TR14 TR17 BCY72 TR18 BCY72 D11 D9 D10 BSX20 TR15 TR16 BSX20 R77 82K R78 27K R79 470 R75 1K R80 4·7K R82 82 R112 1K R11 27K TR19 BSX20 C17 47µ C18 22µ 15V T+C IC64/12 IC40/2

+5V R84 2·2K R85 2·2K R86 33 (CA3046) TR4 R72 22K R73 1K D13 C20 470 R74 100 IC40 SCHMITT TRIGGER

VARIABLE DELAY CHART 1 DISPLAY

SK2 18a TRANSFER PULSE IC43 IC52 S

STROBE PULSE 1 (TO STORES) STROBE PULSE 2 (TO STORES)

SHT 1A RESET 1 (TO COUNTER) RESET 2 (TO OVER RANGE BIST.)

TIME & COUNT GATING LOGIC IC38 IC47 TOT RIIB

C I/p CAMP o/p +5V R76 1K IC36 IC37 C19 470 'EX OR' GATES SN 7486N R83 270 OV

B I/p B AMP o/p +5V R88 1K IC36 IC58 C21 470 R89 270 OV

IC40/5 IC64 IC63 IC73 IC62/2 IC45

MANUAL MANUAL TOP B & C POLARITY SWITCH (REAR VIEW)

INPUT C LOGIC INPUT B LOGIC

F+CR1 P+T F+AVP F+AVP AVP+C T+C IC71 IC72 IC57 IC69 -V +V P̄ C̄ P̄ bf be OV (+V PULSE)+(-V PULSE)+T+C T+C

PIN	POSITION
1	+ PERIOD A
2	- PERIOD A
3	+ PULSE WIDTH A
4	- PULSE WIDTH A

PERIOD A PULSE WIDTH A

FIG. 1 DISPLAY AND LOGIC BOARD - CIRCUIT DIAGRAM E33155

SHEET D. COUNT MODE, RANGES 2 TO 7
(WITH VARIABLE DELAY CIRCUIT)

NOTES

1. INDICATES WIRING POINT
2. SK1 INDICATES CONNECTION TO INPUT AMP BOARD
3. SK2 INDICATES CONNECTION TO BCD/ PROGRAM BD.
4. C-C INCL. ARE 0·01 μF.
5. DE-COUPLING CAPACITORS BETWEEN 0V & +5V.
6. ALL BISTABLES ARE SN7473N UNLESS OTHERWISE STATED (SN74112N, IC)
7. ALL RESISTORS ARE MORGANITE XL 1/4W ± 10% UNLESS OTHERWISE STATED

CHANNEL SELECT I/P2 STOP

SK1 7a 7b 6a 6b 9a 8a 8b 11a 11b

F + CR1 OV

R113 1·5K R114 510 D14 IN4009 C25 S.O.T. −5·2V

R113 510 RESET 3

R116 1·5K R117 510 D15 IN4009 −5·2V

R118 510 IC47/12 (Y)

POLARITY SELECTION GATES

SK1 AMP O/P 9b AMP O/P 10b

R92 1K R93 1K +5V −V +V

IC68 SN74564N P̄ OV

SK1 SK2

12a 27b ag OV

27a ah +5V

13b aj +12V

12b ak −5·2V

14a al Z MOD O/P

P.S. CONNECTIONS

RANGE SELECTION CIRCUIT

SN74151N IC65 RA RB RC RANGE CODE I/P

AVP AVP+C IC49 IC59/6

SN7490N IC44 IC46 IC50 IC53 IC56 IC61 IC66 IC67

TIME BASE (DIVIDER) LOGIC

+5V R69 2·2K TR13 BSX 20 R70 2·2K OVEN SUPPLY

1MHz REF O/p 1MHz (IC34/8)

C15 0·1 XI 10 MHz HIGH STABILITY OSCILLATOR

SN 7490N IC35 1MHz 2MHz

F P+T EXCP EXCP IC38 IC39 IC41 IC54 IC34 IC51 IC60 F+AVP SN74S112N

(+V PULSE)+(−V PULSE)+T+C CONTROL LOGIC

GATE OPEN BISTABLE (F, AVP, MODES) GATE OPEN BISTABLE (P/PW, T, C MODES)

RESET 3 (TO R115) IC49/5 TRANSFER BISTABLE IC48 IC59

+250V R91 150K BTT R90 6·8K TR20 BSX 20 C24 0·1

STOP BISTABLE IC63 IC62 GATE OPEN

RESET BISTABLE IC45/1 IC45/5 IC55 2MHz 1MHz

AUTOMATIC RESET +5V D8 SK2 R C23 64μ 4V C22 100 IC62 IC57

EXT. PROG. TR21 BSX 21 R94 150K BTT R95 6·8K +250V

SWITCH BANK

SK2 IC69 EXCP EXCP H BC

ac R ad R̄ aa R̄ ab R96 4·7K

23a an H̄ 24b ap BC̄ R97 4·7K R98 4·7K

RESET EXT CLOCK HOLD

T̄ 23b aq T̄ R99 4·7K

AVP IC71 25b ar AVP R100 4·7K

AVP IC69 21a as P̄ R101 4·7K

P P̄ IC71 26b at F̄ R102 4·7K

F F̄ IC70 19b au C̄ R103 4·7K

C C̄

TIME AVERAGE PERIOD PERIOD FREQUENCY

RC IC70 20b av RC̄ R104 4·7K

RB IC70 21b aw RB̄ R105 4·7K

RA IC70 22b ax RĀ R106 4·7K

S IC69 22a ay S̄ R107 4·7K

RI IC70 20a az R̄ R108 4·7K

TOT IC70 19a ba TOT̄ R109 4·7K

STORED TOTAL EXT PROG

bb C26 0·1 OV

PROG 25a bc bd +5V R119 1K

IC69 IC63 BC EXCP F+CR1 C P+T T̄ F+AVP F̄ AVP̄ AVP+C C̄ T+C P (+V PULSE)+(−V PULSE)+T+C IC55 IC69 IC72 IC73 -V +V P̄

PERIOD A PULSE WIDTH A

PIN	POSITION
1	+ PERIOD A
2	- PERIOD A
3	+ PULSE WIDTH A
4	- PULSE WIDTH A

VARIABLE DELAY VARIABLE DISPLAY

C16 0·47μ DI2 R71 22K +5V OV IC42 SN74122N (ONE SHOT)

+12V R110 680 DISPLAY RV3 10K R77 82K R81 82K TRI4 TRI7 TRI8 BCY72 BCY72 D11 D9 D10 TRI5 BSX 20 R78 27K R75 1K T+C TRI6 BSX 20 R79 470 C17 0·47μ R80 4·7K R11 27K TRI9 R82 82 BSX 20 C18 22μ 15V IC40 R112 1K T+C

+5V R84 2·2K R85 2·2K TRI4 (CA3046) R86 33 R72 22K R73 1K DI3 C20 470 R74 100

IC64/12 IC40 SK2 180 TRANSFER PULSE IC52 IC43 S

STROBE PULSE 1 (TO STORES) STROBE PULSE 2 (TO STORES)

SHT 1A RESET 1 (TO COUNTER) RESET 2 (TO OVER RANGE BIST.) IC38 IC47 TOT R118 (Y)

SCHMITT TRIGGER TIME & COUNT GATING LOGIC

C I/P CAMP O/P R76 1K C19 470 IC37 R83 270 'EX OR' GATES SN 7486N

B I/P B. AMP O/P R88 1K C21 470 IC58 R89 270 IC40/5 IC64 IC63 IC73

IC62/2 IC45 TOP B & C POLARITY SWITCH (REAR VIEW)

INPUT C LOGIC INPUT B LOGIC

FIG. 1 DISPLAY AND LOGIC BOARD - CIRCUIT DIAGRAM E33155

SHEET E. AVERAGE PERIOD MODE
(WITH VARIABLE DISPLAY CIRCUIT)

NOTES

1. INDICATES WIRING POINT
2. SK1 INDICATES CONNECTION TO INPUT AMP BOARD.
3. SK2 INDICATES CONNECTION TO BCD/ PROGRAM BD.
4. C-C INCL. ARE 0·01 µF.
5. DE-COUPLING CAPACITORS BETWEEN OV & +5V.
6. ALL BISTABLES ARE SN7473N UNLESS OTHERWISE STATED (SN7411 2N, IC)
7. ALL RESISTORS ARE MORGANITE XL 1/4W ± 10% UNLESS OTHERWISE STATED

CHANNEL SELECT I/P2 STOP

POLARITY SELECTION GATES

RANGE SELECTION CIRCUIT

TIME BASE (DIVIDER) LOGIC

HIGH STABILITY OSCILLATOR

TRANSFER BISTABLE

RESET BISTABLE

GATE OPEN BISTABLE (F, AVP, MODES)

GATE OPEN BISTABLE (P/PW, T, C MODES)

STOP BISTABLE

AUTOMATIC RESET

CONTROL LOGIC

SWITCH BANK

VARIABLE DELAY

SCHMITT TRIGGER

TIME & COUNT GATING LOGIC

INPUT B LOGIC

INPUT C LOGIC

B & C POLARITY SWITCH (REAR VIEW)

'EX OR' GATES SN 7486N

P.S. CONNECTIONS

FIG. 1 DISPLAY AND LOGIC BOARD - CIRCUIT DIAGRAM E33155

SHEET F TIME MODE
(WITH VARIABLE DELAY CIRCUIT)

NOTES

1. INDICATES WIRING POINT
2. SK1 INDICATES CONNECTION TO INPUT AMP BOARD
3. SK2 INDICATES CONNECTION TO BCD/ PROGRAM BD.
4. C-C INCL ARE 0·01 μF.
5. DE-COUPLING CAPACITORS BETWEEN 0V & +5V.
6. ALL BISTABLES ARE SN7473N UNLESS OTHERWISE STATED (SN74112N, IC)
7. ALL RESISTORS ARE MORGANITE XL 1/4W ± 10% UNLESS OTHERWISE STATED.

CHANNEL SELECT 1/P2 STOP

POLARITY SELECTION GATES

RANGE SELECTION CIRCUIT

SN74151N IC65

SN74564N IC68

SN74112N

SN7490N

TIME BASE (DIVIDER) LOGIC

OVEN SUPPLY

HIGH STABILITY OSCILLATOR

TRANSFER BISTABLE

RESET BISTABLE

GATE OPEN BISTABLE (F, AVP, MODES)

GATE OPEN BISTABLE (P/PW, T, C MODES)

STOP BISTABLE

AUTOMATIC RESET

CONTROL LOGIC

SWITCH BANK

RESET
EXT CLOCK
HOLD
B - A
B - B
AVERAGE PERIOD
PERIOD
FREQUENCY
COUNT
STORED
TOTAL
EXT PROG

P.S. CONNECTIONS
0V
+5V
+12V
-5·2V
Z MOD O/P

VARIABLE DELAY — VARIABLE DISPLAY

SCHMITT TRIGGER

TIME & COUNT GATING LOGIC

'EX OR' GATES SN 7486N

INPUT B LOGIC

INPUT C LOGIC

B & C POLARITY SWITCH (REAR VIEW)

PIN	POSITION
1	+ PERIOD A
2	- PERIOD A
3	+ PULSE WIDTH A
4	- PULSE WIDTH A

FIG. 1 DISPLAY AND LOGIC BOARD - CIRCUIT DIAGRAM E33155

NOTES

1. INDICATES WIRING POINT
2. SK1 INDICATES CONNECTION TO INPUT AMP BOARD.
3. SK2 INDICATES CONNECTION TO BCD/PROGRAM BD.
4. C-C INCL ARE 0·01 µF.
5. DE-COUPLING CAPACITORS BETWEEN OV & +5V.
6. ALL BISTABLES ARE SN7473N UNLESS OTHERWISE STATED (SN7411 2N, IC)
7. ALL RESISTORS ARE MORGANITE XL 1/4W ± 10% UNLESS OTHERWISE STATED.

CHANNEL SELECT 1/P2 STOP

SK1 7a 7b 6a 6b 9a 8a 8b 11a 11b

F + CRI

R113 1·5K R114 510 D14 IN4009 C25 S.O.T. R113 510 RESET 3

R116 1·5K R117 510 D15 IN4009 R118 510 IC47/12

SK1 AMP o/p 9b AMP o/p 10b

POLARITY SELECTION GATES

R92 1K R93 1K +5V -V +V OV

IC68 SN74564N

SK1 SK2 12a 27b ag OV; 27a ah +5V; 13b aj +12V; 12b ak -5·2V; 14a al Z MOD o/p — P.S. CONNECTIONS

RANGE SELECTION CIRCUIT

IC49 AVP AVP+C AVP IC59/6

SN7415IN IC65 STROBE OV D1 D2 D3 D4 D5 D6 D7 RA RB RC RANGE CODE i/p

TIME BASE (DIVIDER) LOGIC

SN7490N IC44 IC46 IC50 IC53 IC56 IC61 IC66 IC67

IC41 IC38 IC47

+5V R69 2·2K TR13 BSX 20 R70 2·2K IMHz REF o/p OVEN SUPPLY IMHz (IC34/8) OV

C15 0·1 X1 10 MHz HIGH STABILITY OSCILLATOR

F P+T EXCP EXCP IMHz 2MHz IC34 IC39 SN 7490N IC35

IC34 IC51 F+AVP SN74S112N IC55 (+V PULSE)+(−V PULSE)+T+C CONTROL LOGIC

GATE OPEN BISTABLE (F, AVP, MODES) GATE OPEN BISTABLE (P/PW, T, C MODES)

+250V R91 150K BTT R90 6·8K TR20 BSX 20 C24 0·1

RESET 3 (TO R115) IC49S TRANSFER BISTABLE STOP BISTABLE RESET BISTABLE

IC63 IC62 IC48 IC34 OV GATE OPEN +5V IC45/1 IC45/5 2MHz IMHz IC55

AUTOMATIC RESET SK2 D8 R C23 6·4µ 4V OV IC62 IC57 IC57

EXT PROG. TR21 BSX 21 R95 6·8K R94 150K BTT +250V

SWITCH BANK

SK2 IC69 24a am EXCP EXCP; 23a an H; 24b ap BC

R96 4·7K R97 4·7K R98 4·7K

IC71 23b aq T; 25b ar AVP; IC69 21a as P; IC71 26b at F; IC70 19b au C

R99 4·7K R100 4·7K R101 4·7K R102 4·7K R103 4·7K

EXT CLOCK B-C B-B TIME AVERAGE PERIOD PERIOD FREQUENCY COUNT

10^6 10^5 10^4 10^3 10^2 10 1

IC70 RC 20b av RC; RB 21b aw RB; RA 22b ax RA; S 22a ay S; RI 20a az RI; TOT 19a ba TOT

R104 4·7K R105 4·7K R106 4·7K R107 4·7K R108 4·7K R109 4·7K

TOTAL EXT PROG

C26 0·1 PROG 25a bc bd R119 1K +5V

RANGE CODE

R71 22K +5V C16 0·47µ DI2 OV IC42 SN74122N (ONE SHOT)

+12V R110 680 DELAY OR DISPLAY RV3 10K R81 82K TR14 TR17 TR18 BCY72 BCY72 D9 D10 D11 (CA3046) R77 82K R78 27K R79 470 TR15 TR16 BSX 20 BSX 20 R80 4·7K R11 27K R112 1K T+C R72 22K R73 1K TR14 R84 2·2K R85 2·2K R86 33 C17 0·47 C18 22µ 15V TR19 BSX 20 R82 82 IC40 C20 470 R74 100 D13 IC64/12 T+C R75 1K

VARIABLE DELAY VARIABLE DISPLAY SCHMITT TRIGGER

GATE CLOSED GATE OPEN IC40 SK2 18a TRANSFER PULSE S IC43

STROBE PULSE 1 (TO STORES) STROBE PULSE 2 (TO STORES) RESET 1 (TO COUNTER) RESET 2 (TO OVER RANGE BIST.) SHT 1A IC38 IC47 IC47 TOT R118

TIME & COUNT GATING LOGIC

C i/p CAMP o/p +5V R76 1K IC36 IC37 C19 470 R83 270 'EX OR' GATES SN 7486N

B i/p B AMP o/p +5V R88 1K IC58 C21 470 R89 270 IC62/2 IC45

MANUAL MANUAL TOP B & C POLARITY SWITCH (REAR VIEW)

INPUT C LOGIC INPUT B LOGIC

IC40/5 IC64 IC63 IC73 IC63 IC64 IC73 IC40 IC73 IC73 -V +V P

IC63 BC EXCP IC69 PROG 25a bc bd +5V R119 1K

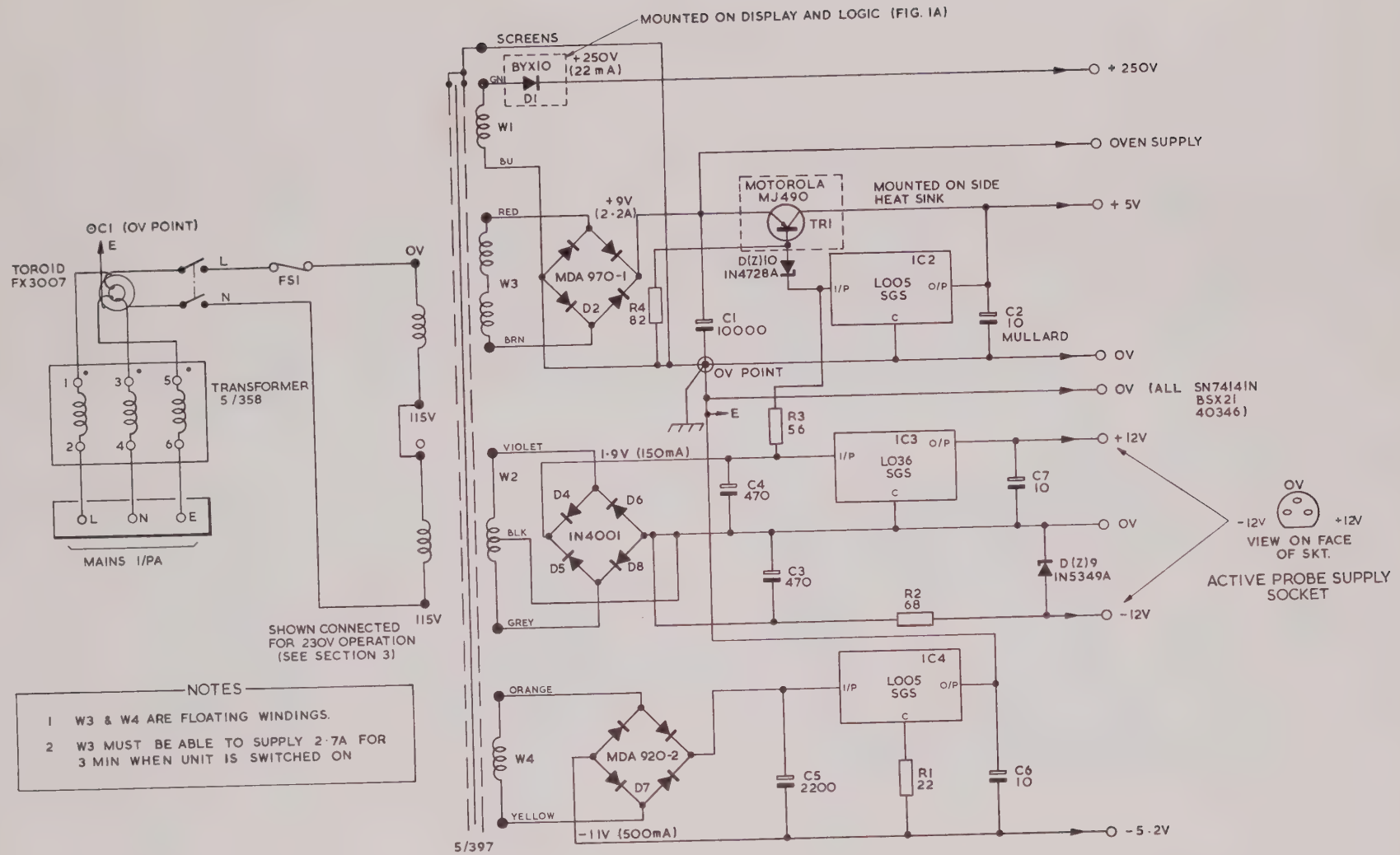
F+CRI IC71 C F+T IC72 T F F+AVP IC72 F AVP F+AVP IC57 AVP+C IC72 C T+C IC55 P OV

(+V PULSE)+(−V PULSE)+T+C IC69 T+C

PIN	POSITION
1	+ PERIOD A
2	− PERIOD A
3	+ PULSE WIDTH A
4	− PULSE WIDTH A

PERIOD A PULSE WIDTH A

FIG. 1 DISPLAY AND LOGIC BOARD - CIRCUIT DIAGRAM E33155



NOTES

1 W3 & W4 ARE FLOATING WINDINGS.

2 W3 MUST BE ABLE TO SUPPLY 2·7A FOR 3 MIN WHEN UNIT IS SWITCHED ON

FIG 6. POWER SUPPLY – CIRCUIT DIAGRAM B.32528/2

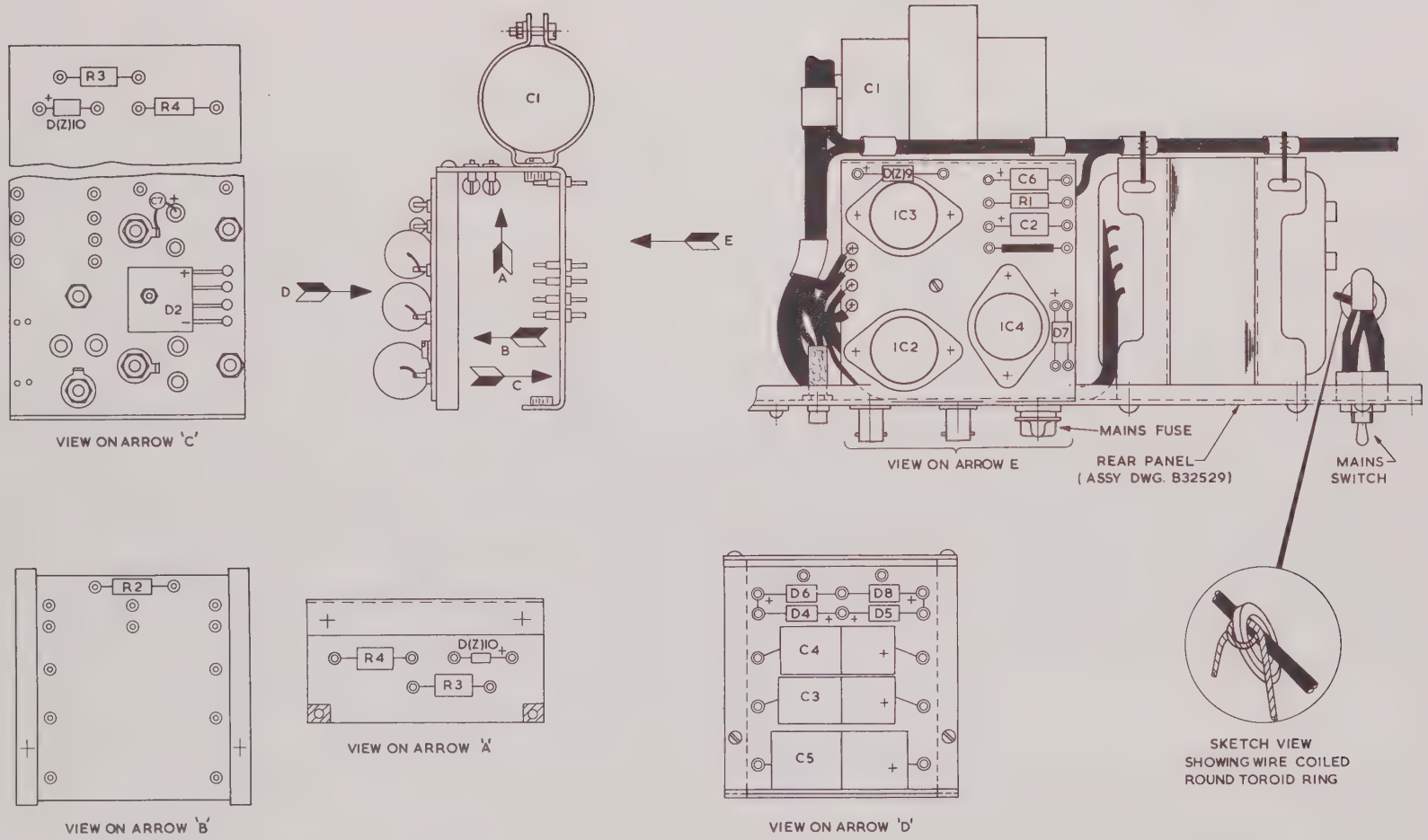


FIG.7 POWER SUPPLY-COMPONENT LAYOUT B32527

BCD FANOUT & PROGRAM BOARD-COMPONENT LAYOUT
OSCILLATOR
X1
SK1
(INPUT AMPLIFIER BOARD)
THIS COMPONENT IS FITTED ONLY ON REQUEST
SK.2
(BCD FANOUT & PROGRAM BD)
DISPLAY AND LOGIC BOARD E.33146/1
SWITCH BOARD B33020/1
RENEWAL INSTRUCTIONS FOR VI-VIO
BOTTOM VIEW OF NUMERICATOR AS SUPPLIED
BOTTOM VIEW OF NUMERICATOR
1 REMOVE MOUNTING SPACER
2 CUT OFF LEAD MARKED No.13 TO WITHIN 1/32" OF BASE OF ENVELOPE (SEE FIG A)
3 RE-FIT SPACER SO THAT LEADS PASS THROUGH SPACER IN CONFIGURATION SHOWN IN FIG B I.E LEADS 2,5 & 11 ARE RE-POSITIONED
4 MOUNT & SOLDER TO P.C. BOARD

FIG. 2 DISPLAY AND LOGIC BOARD, B.C.D FANOUT BOARD AND SWITCH BOARD } COMPONENT LAYOUTS

SENSITIVITY SWITCH	
1	10mV
2	100mV
3	1V
4	10V

INPUT A
1MΩ 20pF
100MHz

O.V. F.P.

INPUT ATTENUATOR

SENSITIVITY

DUAL F.E.T. U257

2N5179

MPS 3640

A.C. AMPLIFIER

OV SIGNAL

SIGNAL

LEVEL

-5·2V

+12V

OV (AMP)

2N5179 TR11 FERRITE BEAD X4

SCHMITT TRIGGER

+5V.

OV (INTERFACE CIRCUITS)

OV (TO COUNTER)

IC1, 3, 4 5, 6, 7 8 & 10

MC1010P

MC1039P

MC1034

1/2 MC1014

1/2 MC1032

MC1013P

MC1010 2P

IC4/3&5

A (R53)

RESET PULSE (PIN 7a)

SK 1

AMP O/P AMP O/P (IC49/8 I/P2) (T+C) TOT IC47/12 (IC62/13) STOP (IC71/8) F+C·RI CHANNEL SELECT '1' '2' '4' RESET '8' '10'

SHEET 1, E33155

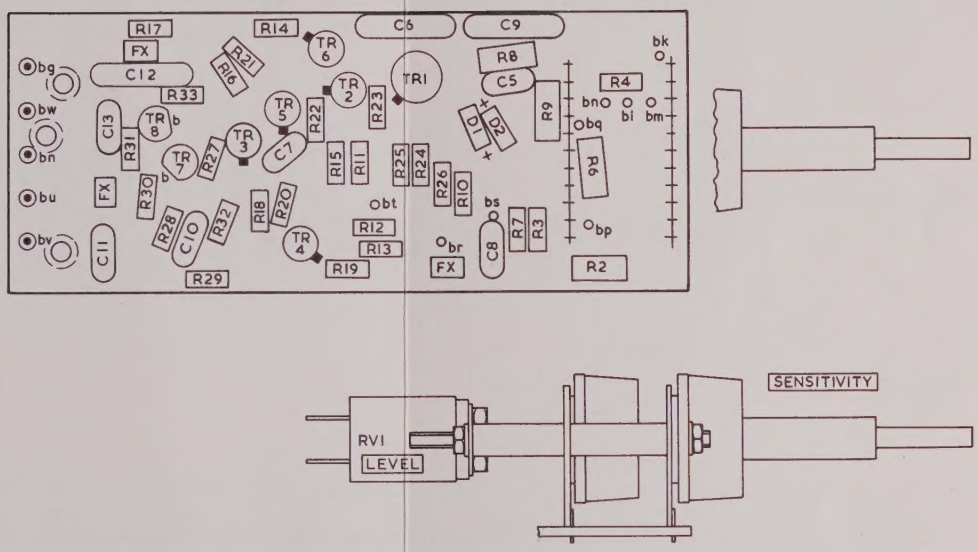
Z MOD O/P

BSX20 TR12

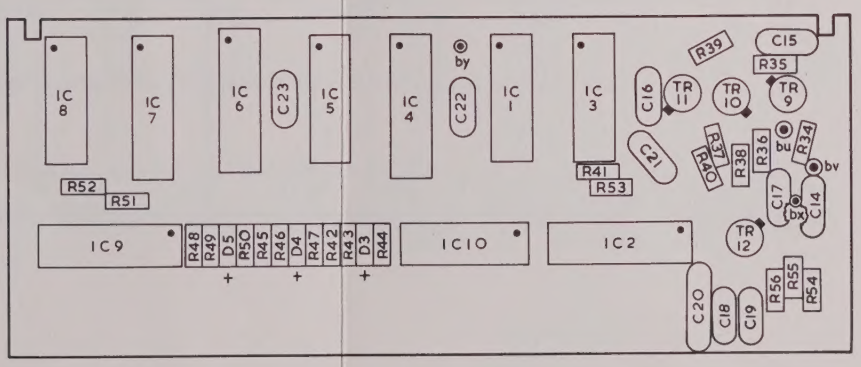
NOTES

1 MC1032 & MC1013: UNUSED INPUTS (J,K̄,S) CONNECTED TO −5·2V.
2 'OR' GATES : MC1039P

FIG. 3 A INPUT AMPLIFIER BOARDS – CIRCUIT DIAGRAM B.33156

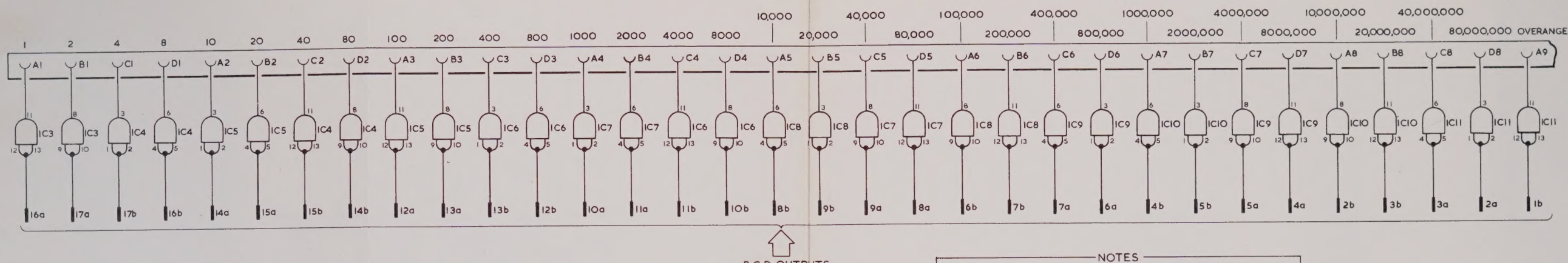


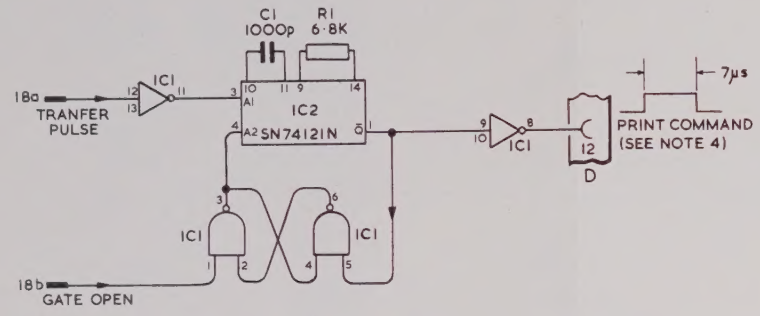
FRONT END D. 33148/1



REAR END D. 33150/1

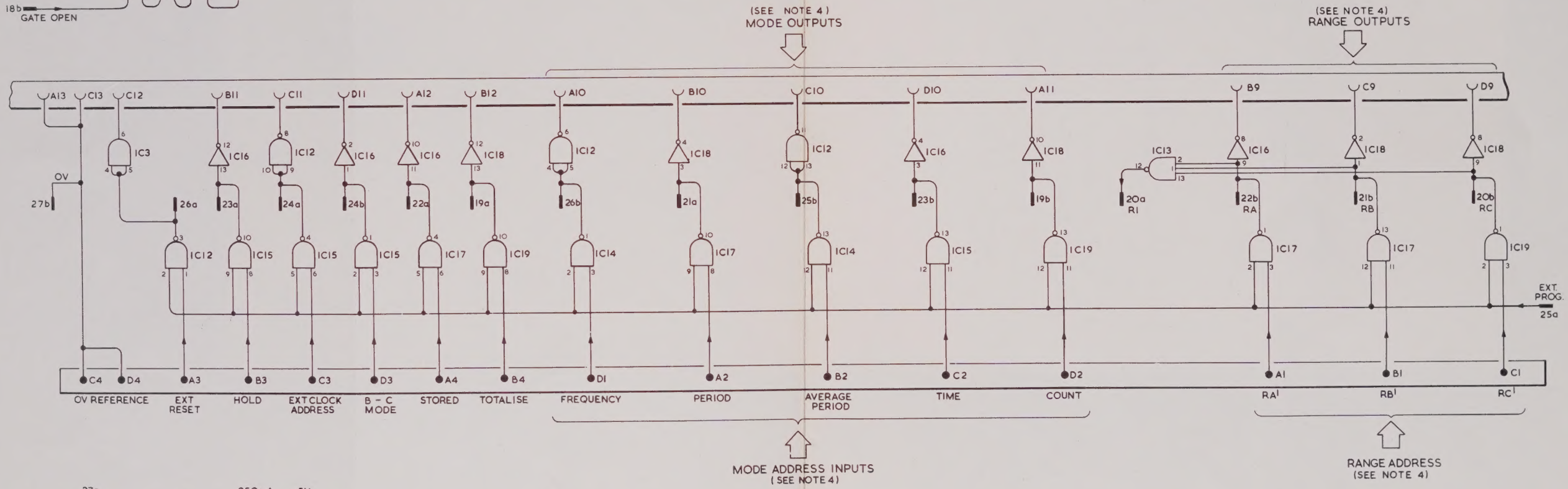
FIG. 4 INPUT AMPLIFIER BOARDS - COMPONENT LAYOUTS





NOTES

1. 7a — DENOTES B.C.D. BOARD EDGE CONNECTOR SK2.
2. D7 — DENOTES PIN CONNECTIONS ON 50-WAY REAR PRINTER OUTPUTS SOCKET.
3. D2 — DENOTES PIN CONNECTIONS ON 18-WAY REAR PANEL EXT. PROGRAM INPUT PLUG.
4. FOR CODES AND / OR LOGIC STATES REFER TO SECTION 3, SUB-SECTION 6.


(SEE NOTE 4) MODE OUTPUTS
(SEE NOTE 4) RANGE OUTPUTS
A13 C13 C12 B11 C11 D11 A12 B12 A10 B10 C10 D10 A11 B9 C9 D9
IC3 IC16 IC12 IC16 IC16 IC18 IC12 IC18 IC12 IC16 IC18 IC13 IC16 IC18 IC18
OV 27b
26a 23a 24a 24b 22a 19a 26b 21a 25b 23b 19b 20a R1 22b RA 21b RB 20b RC
IC12 IC15 IC15 IC15 IC17 IC19 IC14 IC17 IC14 IC15 IC19 IC17 IC17 IC19
EXT. PROG. 25a
C4 D4 A3 B3 C3 D3 A4 B4 D1 A2 B2 C2 D2 A1 B1 C1
OV REFERENCE
EXT RESET
HOLD
EXT CLOCK ADDRESS
B - C MODE
STORED
TOTALISE
FREQUENCY
PERIOD
AVERAGE PERIOD
TIME
COUNT
RA1 RB1 RC1
MODE ADDRESS INPUTS (SEE NOTE 4)
RANGE ADDRESS (SEE NOTE 4)

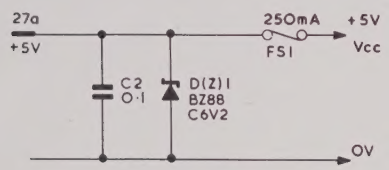


FIG.5 B.C.D. FAN OUT AND EXTERNAL PROGRAMME UNIT SM248

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